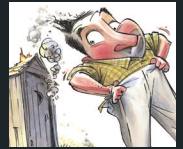


# EDN®

VOICE OF THE ENGINEER

SEPT **17**  
Issue 18/2009  
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Tales from the Cube  
Pg 56

EDN.comment: Robots,  
jobs, and war Pg 6

Baker's Best Pg 18

Tapeout Pg 20

Prying Eyes:  
T-Mobile's G1 Pg 22

Design Ideas Pg 45

## RF SWITCHING OPTIONS: THE RIGHT FIT MIGHT COME WITH A LOSS

Page 30

### BREAKING DOWN THE SENSOR-SIGNAL PATH

Page 25

### IN SEARCH OF A BETTER DRAM: EVOLVING TO FLOATING BODIES

Page 39



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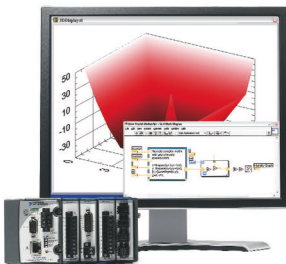


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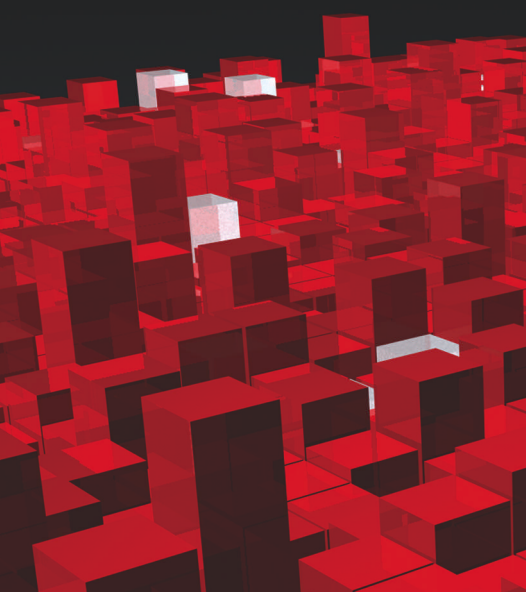
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# EDN 9.17.09 contents

## RF switching options: The right fit might come with a loss

**30** Manufacturers are offering SOI and MEMS alternatives to PIN-diode, GaAs, and electro-mechanical switches for a variety of RF applications, but you need to understand RF-switch specs before you commit to a new technology.

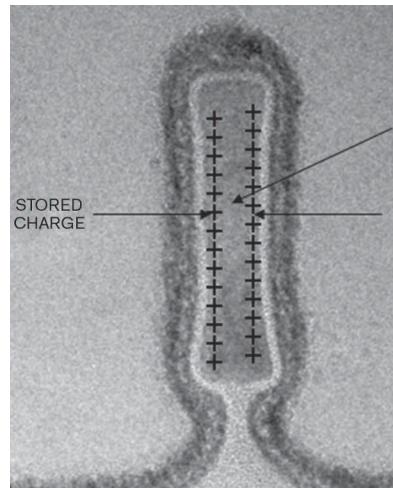
by Rick Nelson, Editor-in-Chief



## Breaking down the sensor-signal path

**25** By understanding the stages of an analog-signal path, digital-system developers can more accurately capture sensor data for a variety of applications.

by Aaron GL Podbelski,  
Cypress Semiconductor



## In search of a better DRAM: evolving to floating bodies

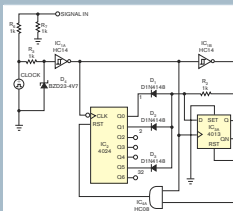
**39** Widely investigated floating-body memories appear to be compelling replacements for conventional DRAMs. A new floating-body memory uses the intrinsic bipolar transistor to store significantly greater charge.

by Serguei Okhonin, PhD,  
Innovative Silicon

## pulse Dilbert 14

- 13** Osram develops direct-emitting green-laser diode
- 13** 1-GHz Cortex-A8 maintains cycle-accurate operation
- 14** Versatile audio analyzer easily quantifies performance of audio components, products
- 14** Mentor unveils strategy at DAC
- 15** Quad 12-bit DAC has internal reference and EEPROM
- 15** Workshop addresses LED challenges
- 16** **Voices:** Newark/Premier Farnell's Gary Nevison: scoping out the Environmental Design of Electrical Equipment Act

## DESIGN IDEAS



- 45** Missing pulse detects position or produces a delay
- 47** Emulate SPI signals with a digital-I/O card
- 48** Resistive DAC and op amp form hybrid divider
- 49** Connect two buttons with just two wires



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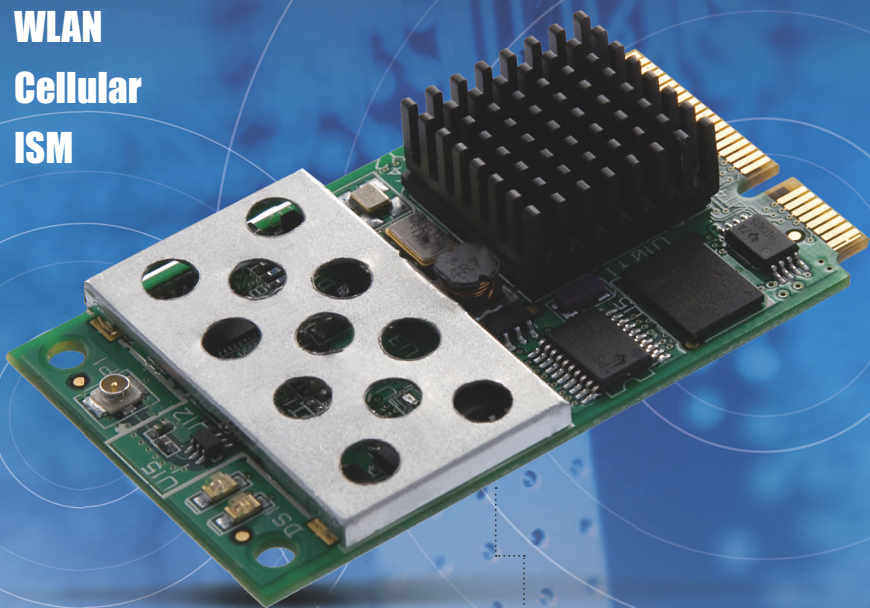
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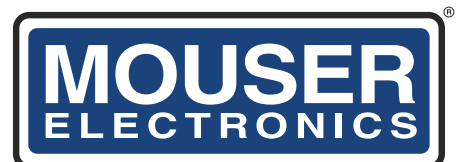


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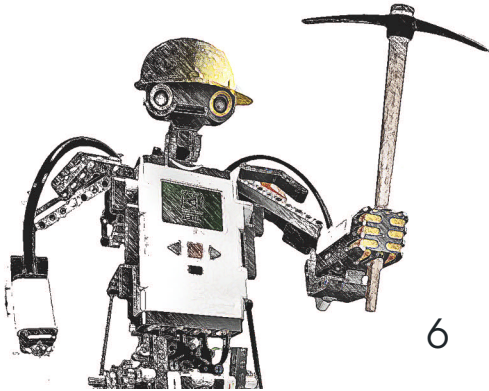
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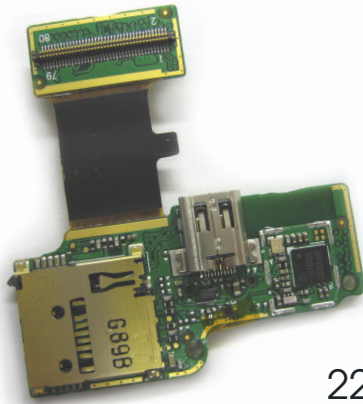


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22

## DEPARTMENTS & COLUMNS

- 6 **EDN.comment:** Robots, jobs, and war
- 18 **Baker's Best:** A designer's guide to op-amp gain error
- 20 **Tapeout:** Reference-tool flows and process-design kits, part one
- 22 **Prying Eyes:** T-Mobile's G1: Google's Android OS emerges
- 53 **Product Roundup:** Power Sources, Integrated Circuits
- 56 **Tales from the Cube:** Lightning strikes sewage setup

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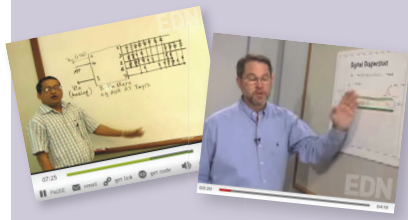
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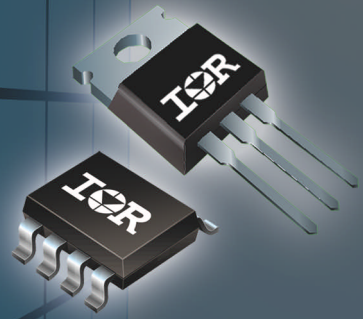
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Gate Drive ±(A)	+1/-4	+2/-7	+1/-4	
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BY RICK NELSON, EDITOR-IN-CHIEF

## Robots, jobs, and war

**R**obotics was a focus of attention at National Instruments' NIWeek event in Austin, TX, last month, when presenters discussed the technical capabilities and ethical considerations surrounding robot use. Although the technical issues got most of the attention, it may be the ethical ones that prove to be more difficult. Consider mining accidents.

Six miners died tragically in the 2007 Crandall Canyon Mine disaster. The loss 10 days later of three would-be rescuers compounded the tragedy. Could the use of robots to perform the rescue reconnaissance have averted those three deaths?

At NIWeek, Thomas Bewley, a professor at the University of California—San Diego, described the challenges robots can face. Those small enough to access a collapsed mine tend to be too small to climb over the debris they encounter once inside. That problem is one Bewley and his students are addressing by finding ways to have small robots climb over large obstacles. A robot should roll when possible, he says, but use multifunction mechanisms, including plungers, for example, when necessary.

It would clearly be ethical to have robots search for survivors in collapsed mines, sparing rescue workers the risk. If such robots can reconnoiter collapsed mines, however, they could take over mining itself. Mining is a dangerous job, but is it better than no job at all? In less dangerous occupations, is it ethical to substitute robots for humans?

In a recent article, Gregory Clark, a professor of economics at the University of California—Davis, doesn't discuss the ethics of the situation but rather the consequences of what he takes to be the inevitable (**Reference 1**). Clark writes that the current downturn is a minor blip in technology-driven economic growth, and, he cautions, "The economic problems of the future will not be about growth but about ... the ineluctable increase in the number of people with no marketable skills and technology's role not as the antidote to social conflict, but as its instigator" as machines displace people.

In a keynote address at NIWeek, David Barrett, PhD, director of SCOPE (Senior Capstone Program in Engineering) at Franklin W Olin College of Engineering (Needham, MA), described robots that are or will be taking over human tasks, including mining, industry, construction, and agriculture. It won't just be unskilled workers who might have something to fear. Barrett also described various medical robots, including ones that perform surgery.

What should we do about robots' displacement of people? Clark pic-

tures a dystopia: "We could imagine cities where entire neighborhoods are populated by people on state support. In France, generous welfare has already produced huge suburban housing estates, *les banlieues*, populated with a substantially unemployed and immigrant population, parts of which have periodically burst into violent protest." To support such populations, he says, "you tax the winners—those with the still uniquely human skills and those owning the capital and land—to provide for the losers."

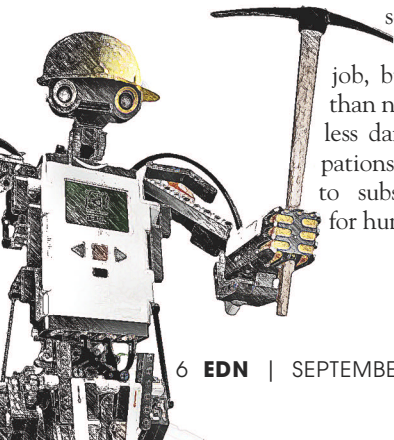
Perhaps the most difficult problem of ethics centers on robots' use in the military. In another recent article (**Reference 2**), James Carroll writes, "When will the unempathetic Americans imagine what it feels like to have a robot monster bolt from the sky—the drones of August—and, in one strike, turn a wedding feast into a funeral?" On the ethics of using robots in warfare, SCOPE's Barrett said that, if we don't do it, our enemies will.

It's inevitable that robots will take on more and more roles. The true ethical question comes into play in how we address the consequences, and so far we have fallen short. We cannot continue turning weddings into funerals and turning middle-class neighborhoods into violent *banlieues* of disaffected, unemployed losers meagerly supported by taxing the winners. **EDN**

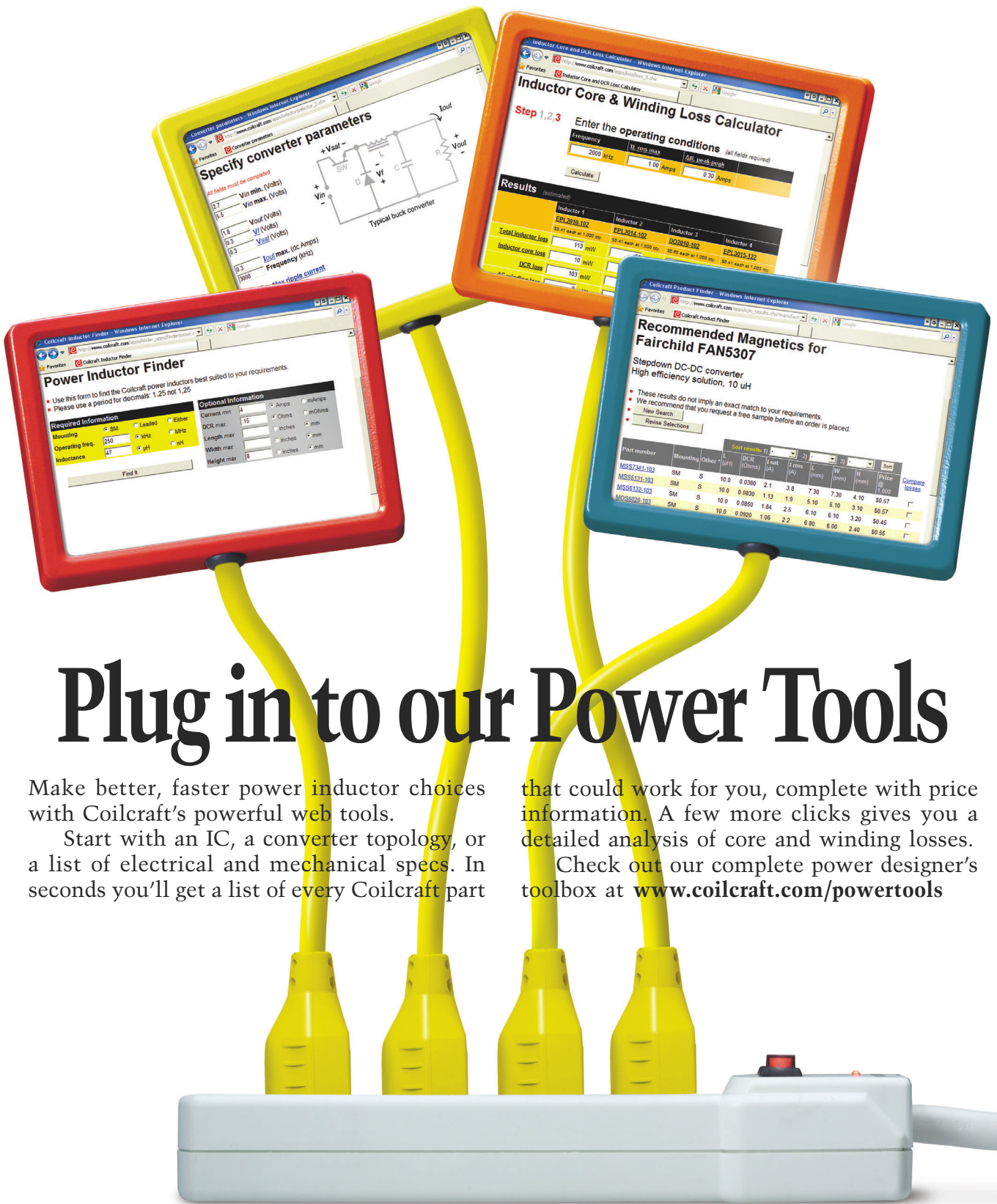
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- 2 Carroll, James, "In search of empathy," *The Boston Globe*, Aug 17, 2009, [www.boston.com/boston\\_globe/editorial\\_opinion/oped/articles/2009/08/17/in\\_search\\_of\\_empathy](http://www.boston.com/boston_globe/editorial_opinion/oped/articles/2009/08/17/in_search_of_empathy).

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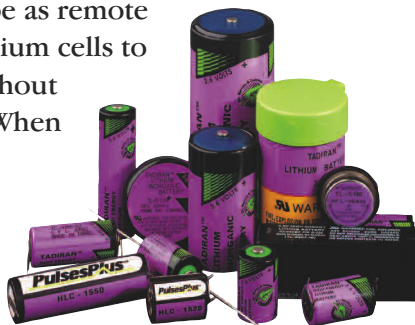
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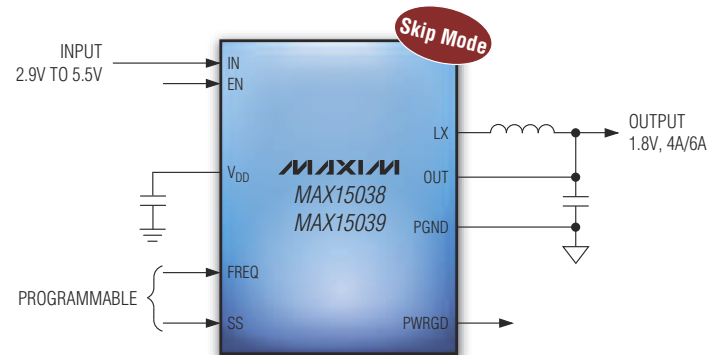
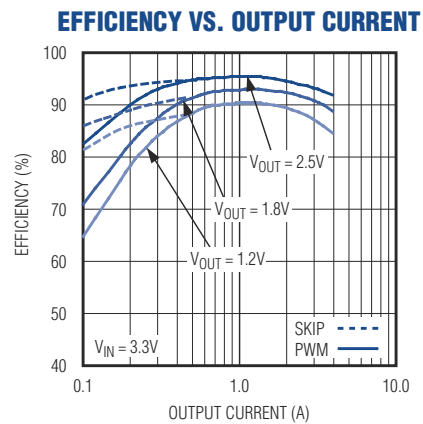
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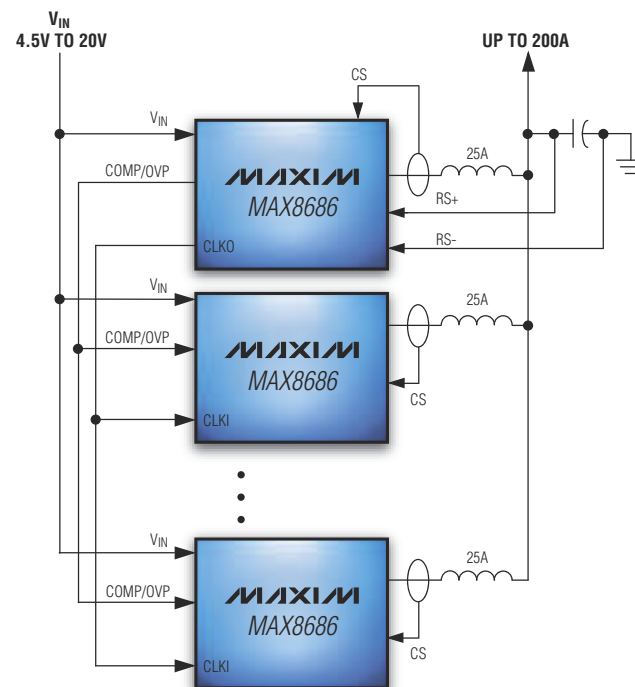
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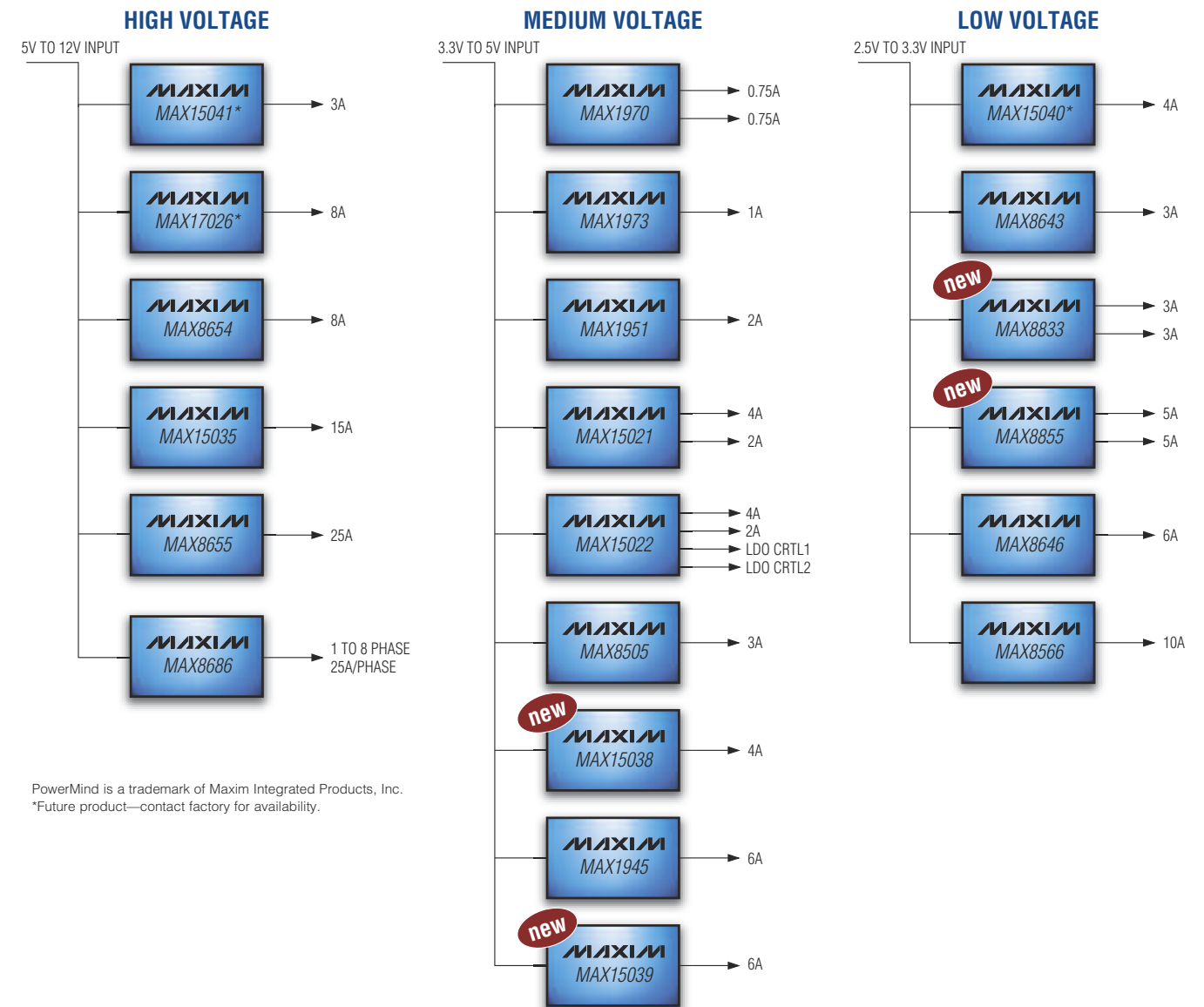


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INNOVATIONS & INNOVATORS

## Osram develops direct-emitting green-laser diode

Osram Opto Semiconductors announced lab results for a direct-emitting green-InGaN (indium-gallium-nitride)-laser diode. In pulsed-mode operation at room temperature, the laboratory prototype achieved an optical output of 50 mW, with a threshold-cur-

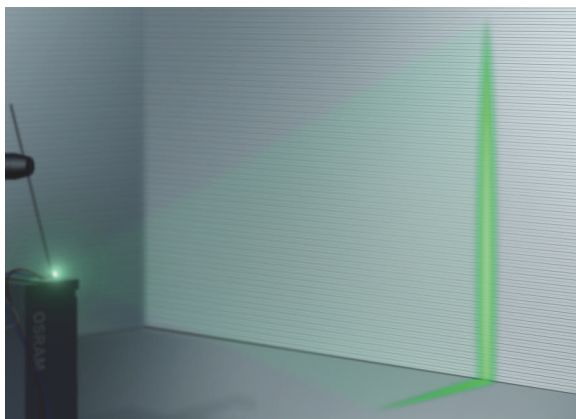
rent density of approximately 9 kA/cm<sup>2</sup>, emitting light in true green—defined by the spectral range of 515 to 535 nm—with a wavelength of 515 nm. The current technology for green semiconductor lasers is to double the frequency of a material capable of lasing at 1060 nm to produce a green laser at 531 nm.

The highest output power for a frequency-doubling green laser is currently about 1.5W.

Osram developed the green-laser diode in conjunction with the German Ministry for Education and Research ([www.bmbf.de/en](http://www.bmbf.de/en)) MOLAS research project, which involves technologies for ultracompact and mobile-laser-projection systems; green lasers also find use in a range of medical and research applications.

—by Margery Conner

▷ **Osram Opto Semiconductors**, [www.osram-os.com](http://www.osram-os.com).



This lab prototype of Osram's direct-emitting green-InGaN-laser diode achieved an optical output of 50 mW in pulsed-mode operation at room temperature.

### FEEDBACK LOOP

**“Einstein, Mozart, and every other genius had contemporaries (and quite smart ones at that) whom they were able to bounce ideas off of and refine their best work. ... Very little would have been discovered if that so-called ‘genius’ were locked in a cell by himself.”**

—Design engineer Chris Gammell, in *EDN's* Feedback Loop, at [www.edn.com/article/CA6666234](http://www.edn.com/article/CA6666234). Add your comments.

## 1-GHz Cortex-A8 maintains cycle-accurate operation

Samsung Electronics and Intrinsicity have worked together to produce an ARM ([www.arm.com](http://www.arm.com)) Cortex-A8 processor, Hummingbird, that can operate at 1 GHz in a 45-nm, low-power process and maintain the same cycle-accurate and Boolean-equivalent operation as the original Cortex-A8 RTL (register-transfer-level) specification. The companies attained this clock rate

by applying custom-designed circuit/memory structures and Intrinsicity's enhanced RTL FastCore and Fast14 high-speed domino logic to timing-critical paths in the Cortex-A8 RTL core. The latest generation of Intrinsicity's NDL (one-of-N-domino-logic) implementation now supports seamless mixing between domino and static logic in a standard-cell-synthesized design. This fea-

ture enables the core to use only those NDL gates that are 25 to 50% faster than static-logic gates in those critical-path circuits in which they affect the overall clock rate. This mixing enables the system to consume less static and dynamic power than earlier implementations of other cores that used the NDL gates throughout the entire core.

The core includes 32-kbyte

instruction and data caches, 512 kbytes of L2 memory, and an ARM Neon multimedia extension. The core supports multiple drain-to-drain-voltage and frequency operation that includes a minimum supply voltage of 1V so that the core can target mobile devices.

—by Robert Cravotta

▷ **Intrinsicity**, [www.intrinsicity.com](http://www.intrinsicity.com).

▷ **Samsung Electronics**, [www.samsung.com](http://www.samsung.com).




## Versatile audio analyzer easily quantifies performance of audio components, products

**A**gilent Technologies has introduced the U8903A audio analyzer, a single unit that incorporates the broad range of capabilities you need to quantify the characteristics that affect sound quality in audio devices. The instrument is also the manufacturer's next-generation replacement for its widely used legacy audio analyzer, the 8903B. The new, scalable, two-channel unit includes several measurement functions and test signals, powerful analysis functions, and industry-standard balanced and single-ended connectors. At dc and from 10 Hz to 100 kHz, the analyzer helps you to measure performance in such applications as consumer and wireless audio and analog-component and -IC test. In ad-

dition, the manufacturer plans to soon offer upgrades that will equip the instrument with as many as eight input channels.

The U8903A offers increased capabilities, wider frequency coverage, and greater dynamic range than the 8903B. The new model also includes a graphical user interface with a 5.7-in. color display and one-button selection of major operating modes. For automated operation, an application note describes equivalent software commands and provides sample test programs that substitute the new unit's SCPI (standard commands for programmable instruments) instructions for the older instrument's commands.

The U8903A is available now at a US list price of \$12,000. For a limited time,

 You can purchase a two-channel analyzer for the price of a typical single-channel unit.

the manufacturer is offering the new instrument at a 20% discount when you trade in an 8903B. With this arrangement, you can purchase a two-channel analyzer for the price of a typical single-channel unit. Find further information about the discount program at [www.agilent.com/find/audioanalyzerpromo](http://www.agilent.com/find/audioanalyzerpromo).

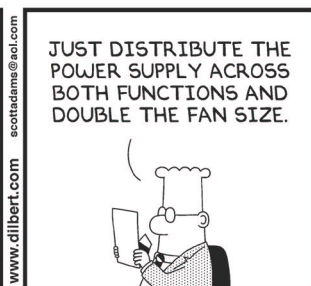
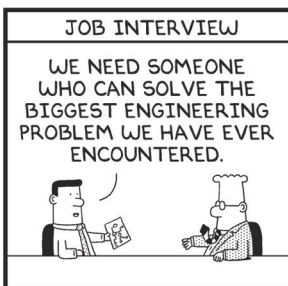
—by Dan Strassberg

► **Agilent Technologies,** [www.agilent.com/find/audioanalyzer](http://www.agilent.com/find/audioanalyzer)



The compact U8903A audio analyzer integrates a range of single-ended and differential source and measurement capabilities that enable you to perform extensive testing of components and systems at dc and at frequencies from 10 Hz to 100 kHz.

### DILBERT By Scott Adams



### MENTOR UNVEILS STRATEGY AT DAC

Mentor Graphics ([www.mentor.com](http://www.mentor.com)) announced its acquisition of Embedded Alley Solutions as a key component of its Android and embedded-Linux strategy last month at the Design Automation Conference in San Francisco. Mentor also announced the integration of its Nucleus graphical-user-interface tool with the ARM ([www.arm.com](http://www.arm.com)) Mali graphics-processing unit; it announced the availability of a Linux/Nucleus operating-system combination for the Marvell ([www.marvell.com](http://www.marvell.com)) Sheeva MV78200 dual-core embedded processor; and it plans to extend Embedded Alley's Android mobile-applications platform to support Freescale Semiconductor's ([www.freescale.com](http://www.freescale.com)) QorIQ and PowerQUICC (quad-integrated-communications-controller) III processors.

Mentor plans to combine its Nucleus RTOS (real-time operating system) and associated tools and services with Embedded Alley's Android and Linux development systems to offer device manufacturers one source for the operating systems they need for embedded-system designs. The goal is to support Mentor's customers in supplying complete systems—not just silicon—to their own customers. For more news on DAC, go to [www.edn.com/090917pulsea](http://www.edn.com/090917pulsea).

—by Rick Nelson

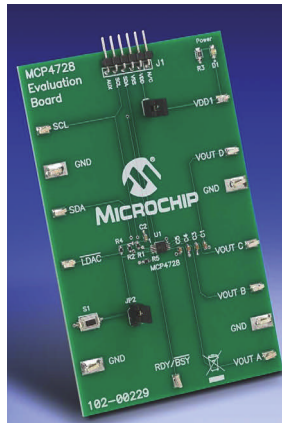
► **Design Automation Conference,** [www.dac.com](http://www.dac.com).

# Quad 12-bit DAC has internal reference and EEPROM

Microchip Technology has announced a quad 12-bit DAC that remembers its settings in an internal EEPROM. The MCP4728 has a  $\pm 2\%$ , 2.048V voltage reference, but you can also use an external reference. The reference has a  $1.2\text{-}\mu\text{V}/\sqrt{\text{Hz}}$  noise floor with a 400-Hz flicker-noise corner. You communicate with the part over an I<sup>2</sup>C (inter-integrated-circuit) bus in standard 100-kbps, fast 400-kbps, and high-speed 3.4-Mbps modes.

You can individually shut down each DAC; total shutdown current is 0.04  $\mu\text{A}$ . You can set the outputs to go to a low-, medium-, or high-impedance state during shutdown. Operating current is 800  $\mu\text{A}$ .

The device features rail-to-rail outputs over the 2.7 to 5.5V power-supply range. Typical DNL (differential nonlinearity)



The MPC4728EV evaluation board interfaces with the \$49 PICKIT serial analyzer, which converts your computer's USB bus to I<sup>2</sup>C, SMBus, SPI, or USART protocols. You can also use your own I<sup>2</sup>C interface board.

is  $\pm 0.2$  LSB with a maximum of  $\pm 0.75$  LSB, which ensures that the device remains monotonic across all input codes. The DAC

contains a power-on circuit for predictable operation.

The device has applications in consumer products, such as personal media players, digital cameras, and GPS (global-positioning-system) devices. Medical applications include portable glucose meters, blood-pressure monitors, and heart-rate monitors. It also finds use in industrial products, such as handheld instruments, motor-control applications, and temperature and light control. The unit's wide temperature range also makes it suitable for automotive applications.

The MCP4728EV evaluation board is available now and costs \$15. The \$1.36 (10,000) MPC4728 operates from  $-40$  to  $+125^\circ\text{C}$  and comes in a 10-pin MSOP.

—by Paul Rako

► **Microchip Technology**,  
www.microchip.com.

**FEEDBACK LOOP**  
“If people want to play in the open-hardware sandbox, they have to share their toys.”

—Robotist Zach Hoeken Smith, in *EDN*'s Feedback Loop, at [www.edn.com/article/CA6676166](http://www.edn.com/article/CA6676166). Add your comments.

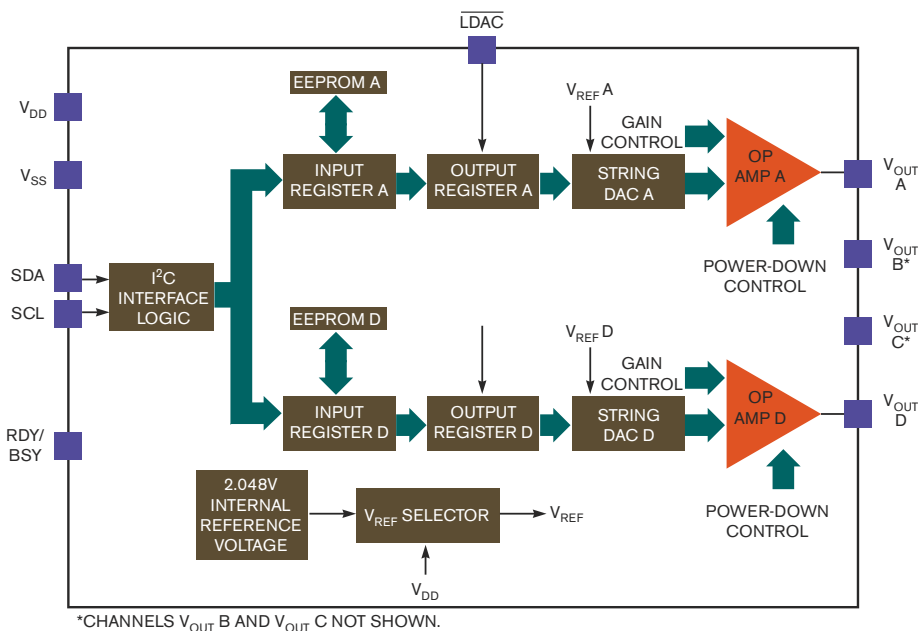
## WORKSHOP ADDRESSES LED CHALLENGES

The US Department of Energy recently invested \$6.4 million in LED design to encourage innovation in solid-state lighting (see [www.edn.com/article/CA6685811](http://www.edn.com/article/CA6685811)). But solid-state lighting is as much about the surrounding electronic-power-control circuitry, thermal management, and optics as it is about the basic LED devices. *EDN* is hosting a free “Designing with LEDs” workshop on Oct 6 at the Westin Lombard hotel near Chicago. The workshop will focus on the electronic-circuit, thermal, and optical-design challenges of designing with solid-state lighting, as well as other LED-based lighting applications. You can register at the Web site below.—by Margery Conner  
► [www.edn.com/leds](http://www.edn.com/leds).

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## Designing with LEDs

In October, *EDN* will host a workshop on designing with LEDs.



You control the Microchip MPC4728 quad DAC with the I<sup>2</sup>C bus. The device's nonvolatile memory allows it to power up without microprocessor supervision.



## VOICES

NEWARK/PREMIER FARNELL'S  
GARY NEVISON:

### scoping out the Environmental Design of Electrical Equipment Act

**A**s a proposed amendment to the 1976 Toxic Substances Control Act, the Environmental Design of Electrical Equipment Act (Bill HR2420) has stirred much controversy within the electronics supply chain about whether a US version of the EU (European Union) ROHS (restriction-of-hazardous-substances) directive is coming. Gary Nevison, legislation and environmental-affairs manager at global Premier Farnell ([www.farnell.com](http://www.farnell.com)) and its US business Newark, recently discussed the bill and compared it with ROHS. The following text includes excerpts from that conversation.

**Is the Environmental Design of Electrical Equipment Act (HR2420), along with the US Toxic Substances Control Act, similar to a US version of ROHS for electronics designers?**

**A** First, this new legislation is clearly not ROHS. It would be misleading to talk about US ROHS compliance. The proposed HR2420 is different from EU ROHS, and, although it is claimed to be legislation designed to control hazardous substances, its main aim appears to be preventing states from imposing substance restrictions on products within the scope of this legislation. It would introduce some limited restrictions, but the exemptions list is so comprehensive that these [restrictions] would be few.

**So, this act is not the US ROHS that many members of the electronics supply chain have been waiting for?**

**A** Initially, this [act] might appear to be so; however, closer scrutiny of the scope and structure of HR2420 reveals that it is ... an effort to limit uncoordinated piecemeal legislation on this issue by individual states. At present, there is no federal US equivalent to EU ROHS, although some states have introduced limited ROHS-like laws. Many manufacturers would welcome a single uniform US ROHS law, as this [law] would remove the need to meet multiple, changing requirements across US states, although others, which predominantly sell internally, may be concerned about this extra restriction.

The main implications of HR2420 are for new chemicals or major new uses of existing ones. For example, products containing substances that are not included in the TSCA [Toxic Substances Control Act] register require certification before they can be imported. TSCA



currently imposes very few restrictions on substances, but it does affect lead-based paints, asbestos, and polychlorinated biphenyls.

**Please elaborate on how HR2420 differs from ROHS.**

**A** Although the bill proposes to restrict the same six substances as EU ROHS at the same concentration values in homogeneous materials, there are no apparent equivalents to 17 EU ROHS exemptions, and there is no use of the EU ROHS product categories. The product scope appears quite different from EU ROHS, as it seems to exclude household or consumer products and include products not covered by EU ROHS, such as electricity-distribution equipment. Another significant difference is that EU ROHS excludes products designed for use with voltages above 1000V ac or 1500V dc, whereas HR2420 has a limit of 300V. The restrictions would apply to products manufactured after July 1, 2010.

So, in summary, the scope of the bill is quite limited and is clearly different from EU ROHS and mainly consists of a detailed list of exclusions and exemptions. As the scope includes many items currently excluded from EU ROHS, HR2420 does not appear to be a federal ROHS bill—more

an attempt to avoid disjointed ROHS requirements emerging for products currently outside or on the fringe of the scope of EU ROHS.

**Many engineers think that, once the original ROHS hubbub concluded, all of the environmental compliance issues were behind us. Why is it important for engineers and OEMs to continue to work with distributors on environmental compliance issues?**

**A** That [ending of controversy] was never the case. Under the original ROHS scope, it was always going to be reviewed, there were always going to be more substances, product categories, etcetera. And now we have the REACH [registration/evaluation/authorization-of-chemicals] directive. There will be more and more and more products and substance [limitations] in the short, medium, and long term, [which] will probably be the biggest issue for design engineers around the world. They will have to seek suitable alternatives to these ever-increasing [number of] substances. This [situation] is kind of a nightmare. It is going to roll and roll and roll for many years.

Sure, engineers could look at all of this on the Web, but there is so much information and so much misinformation that is now dated that a distributor is a good route to take. There are good distributors doing this [work] and there are not so good, but one of the biggest issues for me is whether things ever get deleted from the Web. For the designer, the simple reason would be getting the latest information, providing the distributor is doing the job well. —interview conducted and edited by Suzanne Deffree

# Rarely Asked Questions

Strange stories from the call logs of Analog Devices

## What's the (Converter) Frequency Kenneth?

**Q.** How Do I Design a Converter Front-end without Compromising the Performance?

**A.** Designers that employ a converter for high-frequency sampling have to face many challenges. Designing a front-end isn't simple, but the following comments can guide the designer to a solution.

Designers can choose amongst three types of front-ends: baseband, narrow-band, or wideband; the application determines which should be applied.

Baseband applications require bandwidth from dc or the low MHz to the Nyquist frequency of the converter. In terms of relative bandwidth, this implies about 100 MHz or less. These designs can employ either an amplifier or a transformer (balun).

Narrowband applications (narrow being relative to the ADC's full Nyquist bandwidth) usually operate at high intermediate frequencies (IF). They typically use only 5 to 20 MHz of bandwidth in the 2nd or 3rd Nyquist zone, with a center frequency  $\geq 190$  MHz. The design only needs a portion of the Nyquist bandwidth, but the unused bandwidth is often needed to implement an anti aliasing filter. A transformer or balun is typically used for these applications, but an amplifier can be used if its performance is adequate at these frequencies.

Wideband designs need it all, with the user taking as much as the converter will supply. These designs have the widest bandwidth, making the front-end design the most challenging of the three types. These applications require bandwidth from dc or low MHz to several GHz. Currently, these designs



typically employ a wideband balun, but amplifiers are catching up in bandwidth and performance.

After choosing the converter, choose the front-end amplifier (active) or transformer (passive). The tradeoffs between the two are many and depend on the application, but can be distilled to a few points. Amplifiers add noise, require a power supply, and burn power, but they are not gain bandwidth dependent like a transformer. Also, they have better gain flatness within the pass band region. Transformers are passive, so they don't add noise or burn power, but their asymmetrical behavior can cause spurious issues. Transformers are not ideal devices; if not used properly their parasitics can undermine any design, particularly at higher frequencies ( $>100$  MHz).

Hopefully, this advice will keep the design on track. For additional information, please refer to the references or send me an email.

**To Learn More About  
Front-end Design**

<http://designnews.hotims.com/23118-101>



**Contributing Writer**  
Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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BY BONNIE BAKER



# A designer's guide to op-amp gain error

**A**s you sit down to select the proper operational amplifier for your circuit, the first order of business is to determine the signal bandwidth that your system will send through that amplifier. Once you settle on this parameter, you can start to look for the right amplifier. The high-speed-op-amp gurus warn that you should avoid using analog devices that are too fast for your application. So you try to pick an amplifier with a closed-loop bandwidth just a little higher than the maximum frequency of your signal.

This strategy may sound like a good product-selection recipe, but it will probably bring disaster to your application board. In the lab, you may find that, when you put an input-sine-wave signal at the application's maximum frequency into your system, the output signal from your amplifier does not go across the expected full-scale analog range. The gain on the signal is much less than you would expect. If the slew-rate magnitude of your amplifier is more than adequate and you are not driving the amplifier output into the power-supply rails, then what has gone wrong?

Stop double-checking your resistor values! When designing an amplifier into a gain cell, you must know your signal's maximum bandwidth, the amplifier's closed-loop noise gain, the amplifier's gain-bandwidth product, and how much gain error your design can tolerate. The closed-loop noise gain is the amplifier's gain, as if a small voltage source were in series with the

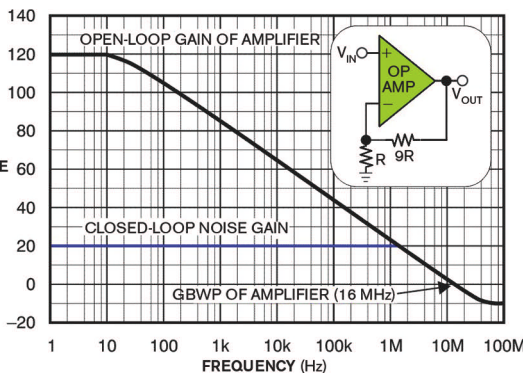


Figure 1 The open- and closed-loop gain of this voltage-feedback amplifier has a gain-bandwidth product of 16 MHz and a circuit noise gain of 10V/V.

op amp's noninverting input.

You can work this problem through by example. For instance, start with a signal bandwidth of 1 MHz. The amplifier's circuit noise gain in Figure 1 is 10V/V. Figure 1 also shows the open-loop frequency response of an amplifier that has just enough bandwidth for this circuit—or so you think. The amplifier has a 16-MHz gain-bandwidth product. The op amp looks as though it can support a gain

of 10V/V, or 20 dB, out to 1 MHz, but look a little closer. The gain of the open-loop gain curve at the signal's bandwidth is

$$A_{OL-SBW} = \frac{GBWP}{SBW},$$

where  $A_{OL}$  is the open-loop gain of the amplifier,  $SBW$  is the signal bandwidth, and  $GBWP$  is the gain-bandwidth product.

In this case, the amplifier's open-loop gain,  $A_{OL-SBW}$ , is 16V/V at 1 MHz. But here's the kicker: The closed-loop gain error in this circuit is  $NG / (A_{OL-SBW} + NG)$ , where  $NG$  is the noise gain. The closed-loop gain error at 1 MHz in this example is 0.385, or a gain error of 38.5%.

For this circuit, if you are willing to tolerate a gain error of 0.05 from your amplifier and you understand that the  $GBWP$  of an amplifier can change a maximum of 30% from product to

product and over temperature, you need an amplifier that has a  $GBWP$  greater than 246 MHz. The guiding formula is

$$GBWP_{OPA} = 1.30 \times \frac{NG \times SBW \times (1 - ERROR)}{ERROR},$$

where  $GBWP_{OPA}$  is the op amp's gain-bandwidth product.

Use this formula during your first pass when you choose an amplifier for your circuit. After you determine the amplifier's bandwidth, you can start to delve into

the other important amplifier characteristics for your application. **EDN**

## REFERENCES

- 1 Bendaoud, Soufiane "Gain error affects op amp choices," *Planet Analog*, July 14, 2006, [www.planetanalog.com/features/analog/showArticle.jhtml?articleID=190400337](http://www.planetanalog.com/features/analog/showArticle.jhtml?articleID=190400337).
- 2 Mancini, Ron, "Op-amp-gain error analysis," *EDN*, Dec 7, 2000, [www.edn.com/article/CA56190](http://www.edn.com/article/CA56190).



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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

## Reference-tool flows and process-design kits, part one

**M**ost of the advanced process technologies from wafer foundries include RTFs (reference-tool flows) to aid in tool selection. In addition, PDKs (process-design kits) describe the electrical, yield, and performance aspects of the process. These two pieces of support documentation have been the basis of chip design since the start of the semiconductor industry. Although these files provided adequate information for engineers to complete designs on process geometries as small as 0.25 micron, they alone do not represent all of the issues that lithographic and advanced processing variation introduces.

An RTF is usually a sequence of recommended tools that identify all of the steps—with the associated EDA tools—you need to verify that a physical-design view of a circuit meets all of the quality criteria to ensure manufacturability. The RTF also ensures that the chosen EDA tool will operate with the information the foundry provides and produce a “correct” result. Most of these tool flows involve timing closure and detailed placement and routing of the circuits—capabilities that all of the major EDA vendors provide. Supplementary tools include device simulators; parasitic RC (resistance/capacitance) extractors; physical verification, including DRC (design-rule checking), LVS (layout versus schematic), and ERC (electrical-rule checking); package modeling; high-capacity simulation; noise modeling; power analysis; and custom layout. The addition of these supplementary tools allows customers who want analysis outside their all-in-one flow to add independent checks or advanced analysis.

**Most fabs try to maintain more than 2000 control files for a commercial-foundry offering, so updates take time, and the customer must verify them.**

A key misunderstanding about the tools in RTFs is that the foundry advocates them. Rather, the RTF is a list of tools with known interoperability with each other. Furthermore, the foundry believes that these tools can produce a result from a certain level of publicly released information on the process within an acceptable amount of error that the wafer foundry determines. Participation in an RTF does not guarantee correct answers from any EDA tool for an arbitrary circuit application, so don't blindly trust the tools on the list. As a corollary, omission from the

list merely indicates that the foundry has not established vendor-to-vendor interoperability from a menu level or that, to achieve higher accuracy or performance, the tool requires supplemental information that is not available to the general design community but may be available on a case-by-case basis. Typically, mixed-signal, RF, memory, imaging, telecom, very-high-speed, multiprocessor-core, DSP, and low-power designs do not use RTFs.

The basics of RTFs are the technology files that describe the masking and design layers for the process and their functions. This technology also contains a naming convention and information for operating a custom physical-design tool, or layout editor. The technology file also has the rudimentary minimum-design-rule information for the process, so physical-system designers can use the rules as guidelines. There is also a place-and-route control file, which dictates device-to-device and wire-to-wire spacing on the design and is written in the dialect of the EDA vendor's tools.

The last major component is the physical-verification files. These files include the DRC deck, which comprises minimum rules, recommended rules, DFM (design-for-manufacturing) “increased-yield” rules, memory rules, I/O rules, power-supply rules, ESD (electrostatic-discharge) rules, analog rules, and special-device rules. A similar format is available for ERC-, LVS-, and parasitic-extraction-rule decks. As a result, most fabs try to maintain more than 2000 control files for a commercial-foundry offering, so updates take time, and the customer must verify them. **EDN**

Contact me at [pallabc@siliconmap.net](mailto:pallabc@siliconmap.net).

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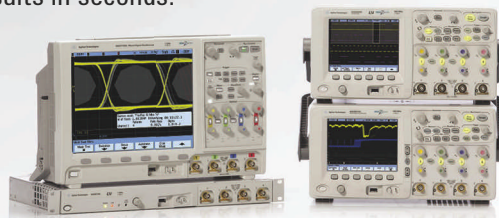


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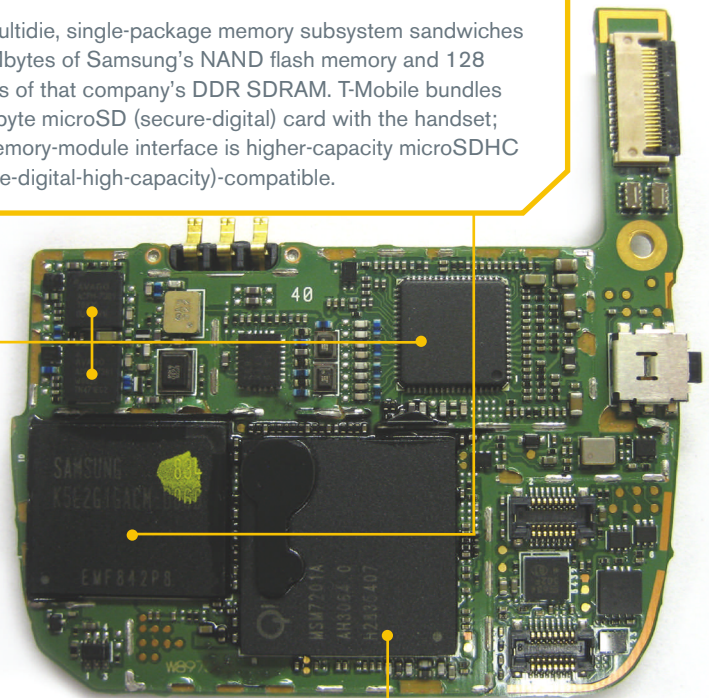


# T-Mobile's G1: Google's Android OS emerges

The myTouch 3G (also known as the HTC Magic), T-Mobile's second Google Android-OS-based and HTC-designed handset, recently became available for purchase. More svelte and with a more responsive touchscreen than its predecessor, the G1 (also known as the HTC Dream), the myTouch 3G conversely relies exclusively on an on-screen virtual keyboard. After peeling away the G1's oft-preferred physical keyboard, my Prying Eyes partners at phoneWreck discovered some interesting facts about the two primary PCBs (printed-circuit boards) inside the premier Google Android offering.

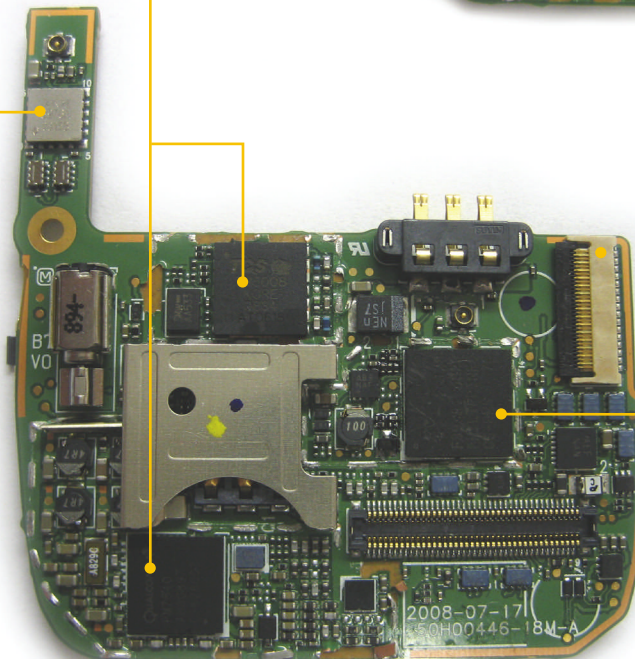
T-Mobile's UMTS (Universal Mobile Telecommunications System) cellular-data network leverages the WCDMA (wide-band-code-division/multiple-access), 1700- and 2100-MHz bands in the United States, whereas GSM (global-system-for-mobile)-communication competitor AT&T, which currently touts a more extensive 3G coverage footprint, employs 850- and 1900-MHz spectrum slices. You'll therefore see some unique pieces of silicon in the G1 versus, say, the BlackBerry Bold (see "Trolling for gold in the BlackBerry Bold," *EDN*, May 28, 2009, pg 20, [www.edn.com/article/CA6659415](http://www.edn.com/article/CA6659415)). Avago's ACPM-7381 and ACPM-7391 UMTS power amplifiers, along with TriQuint's ALM-1412 quadband power-GSM amplifier, together mate to Qualcomm's RTR6285 RF transceiver and PM7540 power-management IC. Avago also supplies the ALM-1412 GPS (global-positioning-system) amplifier.

The multichip, single-package memory subsystem sandwiches 256 Mbytes of Samsung's NAND flash memory and 128 Mbytes of that company's DDR SDRAM. T-Mobile bundles a 1-Gbyte microSD (secure-digital) card with the handset; the memory-module interface is higher-capacity microSDHC (secure-digital-high-capacity)-compatible.



AKM's AK-7986A six-axis electronic compass supplements the G1's accelerometer and GPS capabilities to provide the handset with a rich set of location, motion, and direction statistics.

Qualcomm's 528-MHz MSM7201A baseband processor, which embeds GPS and audio DAC/ADC functions, acts as the brains of the G1. Curiously, HTC augmented the G1's logic with a Xilinx XC2C128 CoolRunner-II CPLD, which HTC has also employed in past PDA and smartphone designs. Although the CPLD seemingly runs counter to the integration- and cost-optimized focus of a high-volume consumer-electronics device, it also enables HTC to easily augment and update hardware capabilities both on the manufacturing line and in the field.

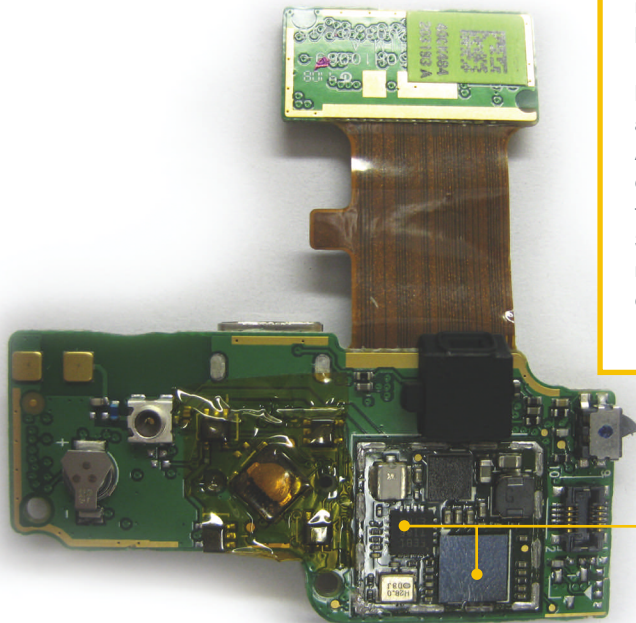


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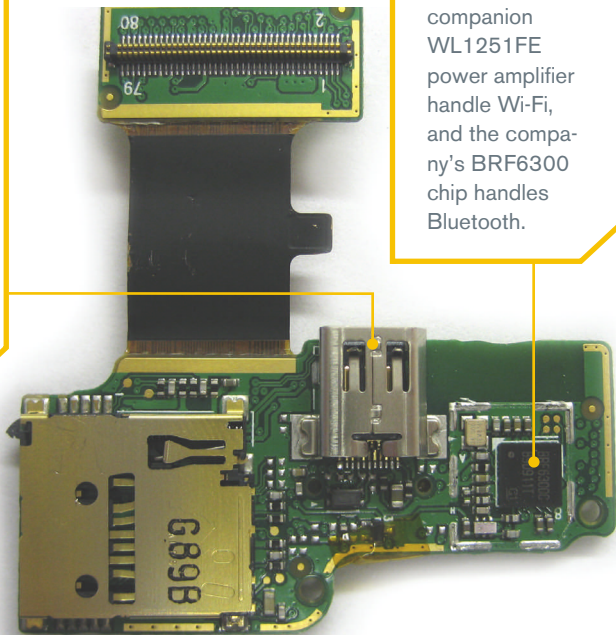


Not shown are the G1's 3.2M-pixel still-image-only camera based on Aptina's (formerly Micron's) MT9T013D sensor and Analog Devices' AD5398 autofocus-capable lens-coil driver; the Sharp-supplied 3.2-in., 320×480-pixel-resolution and 65,536-color LCD; and the 1150-mAhr battery.



The device has 802.11b/g Wi-Fi- and Bluetooth-connectivity options. The Texas Instruments WL1251B transceiver and companion WL1251FE power amplifier handle Wi-Fi, and the company's BRF6300 chip handles Bluetooth.

For those of you who prefer old-fashioned but reliable wires, SMSC's (Standard Microsystems Corp's) USB3316 USB (Universal Serial Bus) controller has you covered.



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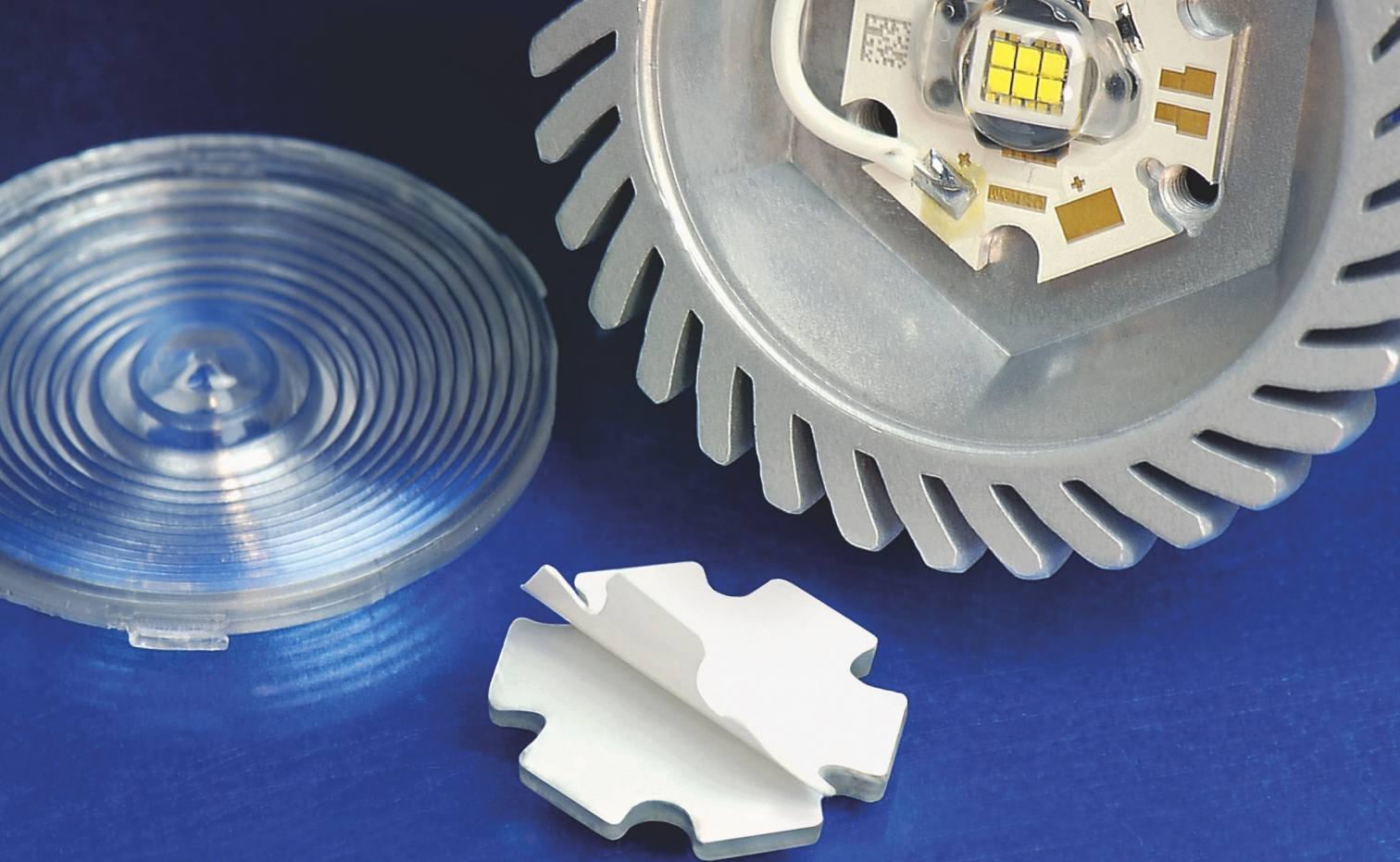
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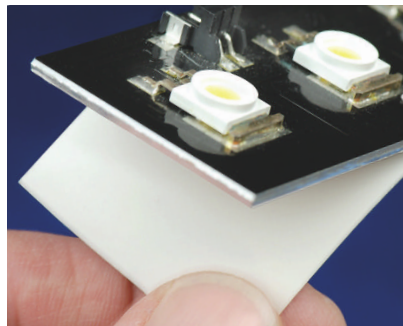
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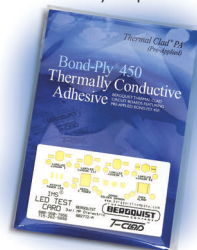


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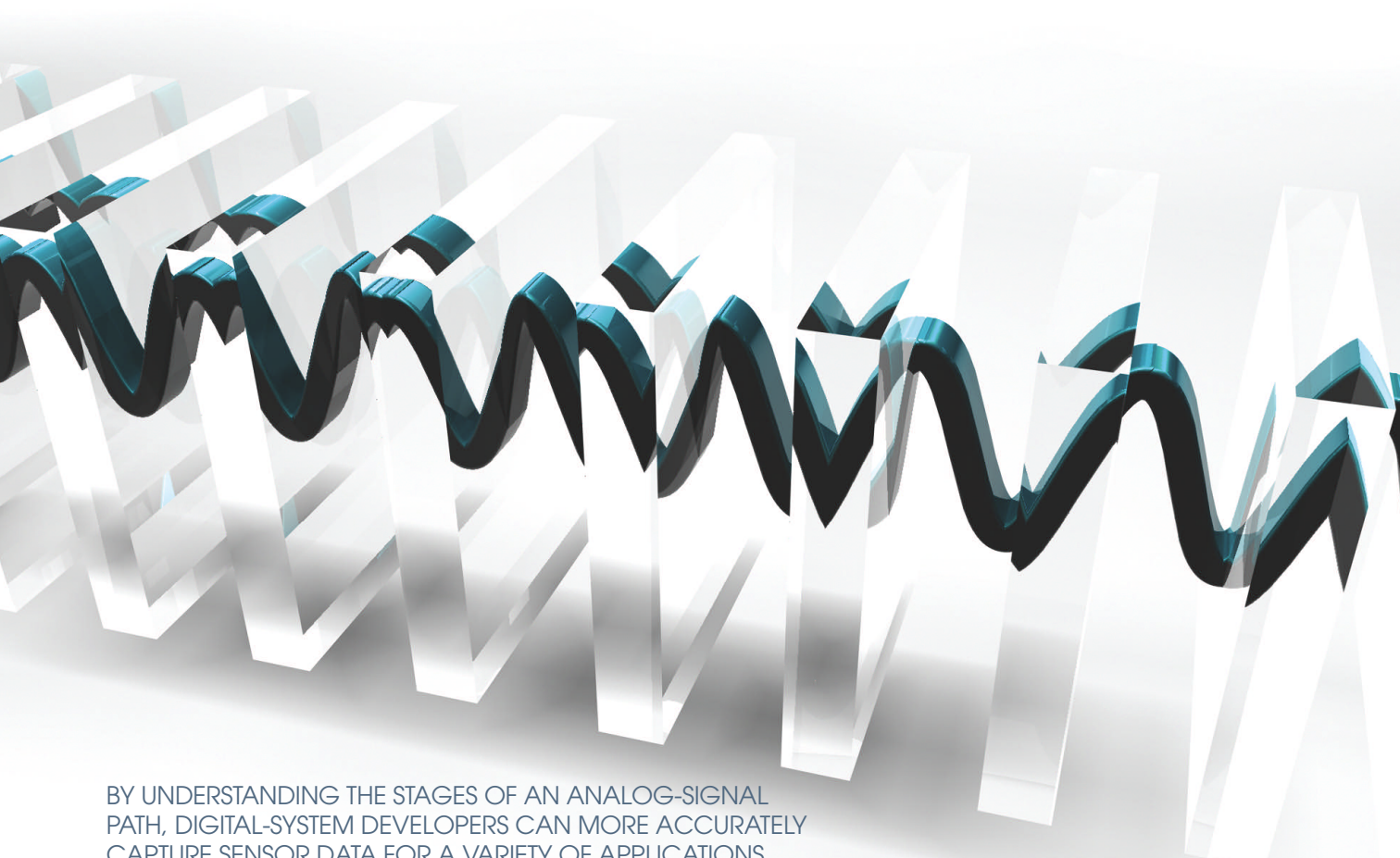
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BY UNDERSTANDING THE STAGES OF AN ANALOG-SIGNAL PATH, DIGITAL-SYSTEM DEVELOPERS CAN MORE ACCURATELY CAPTURE SENSOR DATA FOR A VARIETY OF APPLICATIONS.

# BREAKING DOWN THE SENSOR-SIGNAL PATH

BY AARON GL PODBELSKI • CYPRESS SEMICONDUCTOR

**S**ensors are increasingly finding use in embedded systems. Although industrial products have long used them for manufacturing-control systems, consumer devices are now starting to employ them, as well. Manufacturers are integrating sensors into consumer products to create better user experiences—ranging from adding accelerometers in mobile phones to adding water-vapor sensors in microwave ovens. System designers, who previously worked only in the digital domain, are now finding themselves having to interface with analog sensors.

You must digitize a sensor's analog signal so that the system can use it, and the signal path goes through amplification,

filtering, and digitization stages (Figure 1). Each stage usually involves a component with passives around it to perform properly for an application. Once you digitize the signal, you can pass it to

a control system on the microcontroller or massage the data and pass it to a host processor through a communication protocol. The protocol can use the sensor data as necessary.

Every sensor has a different output signal and range. The output signal can be voltage-, current-, resistive-, capacitive-, or frequency-based, but few standards exist, and only specific industrial systems use them. Even similar sensors from the same manufacturer can have different outputs, and these differences can create problems for system designers. A designer must select a sensor that meets the requirements for the system. If the requirements change during the design, however, a sensor change may also be in order. In addition, a new sensor with a slightly different output would necessitate altering the amplification and filtering stages.

Most sensors output a low-level current- or voltage-based signal, so a simple resistive network adapts any current-based signal into a voltage. This article





simplifies some concepts and the component-selection process.

## AMPLITUDE

The output of a sensor can be as small as several millivolts or as large as several volts. For proper digitization, the signal must be large enough for the ADC to effectively read it. In most cases, the sensor signal requires amplification. For example, a typical type-K thermocouple outputs  $41 \mu\text{V}/^\circ\text{C}$ , which you must greatly amplify if your design requires  $1^\circ\text{C}$  granularity. Thus, you must take ADC resolution into account to ensure that you sufficiently amplify the signal to obtain the desired granularity.

You base the selection of an amplifier mainly on the type you need—be it an instrumentation amplifier, a differential amplifier, an operational amplifier, or a PGA (programmable-gain amplifier). You also must determine the amount of gain your amplifier requires. A resistive network, with feedback, around the amplifier sets the amplifier's gain. The maximum gain for standard amplifiers is ideally limitless. A digital signal to the device usually sets the gain for a PGA. This signal alters an internal resistive network. The maximum possible gain for a PGA is 0.5 to 1000 times less than that of a traditional amplifier, but this range is more than acceptable in most cases.

### AT A GLANCE

Even similar sensors from the same manufacturer can have different outputs, and these differences can create problems for system designers.

Noise arises from a number of sources, including board layout, radios, thermal components, and even the sensor itself.

To use the sensor's filtered signal, you must quantify the analog signal into the digital domain using an ADC.

You have the choice of using an external ADC or a microcontroller with an integrated ADC. External ADCs tend to have higher accuracy and higher performance in both speed and resolution.

With amplifiers, you must take into account another key specification: offset voltage. Offset voltage is the amount of alteration in volts of a signal that passes through the amplifier. For example, if you put a 500-mV signal into an amplifier with unity gain, or a gain of one, and an offset voltage of 10 mV, the resulting output would be 510 mV. If the output range of the sensor is 0 to 900 mV and the system does not need a very granular reading of the sensor, this offset may be negligible. If the range of the sensor

is 450 to 550 mV, this offset is probably unacceptable. The smaller the offset voltage, the more costly the amplifier is. All amplifiers have an offset, but you need to know whether the system can tolerate it. You can reduce or eliminate the offset voltage using correlated double sampling.

## FILTERING

All systems impart some noise on the sensor's signal. Noise arises from a number of sources, including board layout, radios, thermal components, and even the sensor itself. Signal noise causes the ADC to make inaccurate and unstable readings, and the noise level increases through the amplification stage, which exaggerates the error in the signal. You can qualify signal noise as low frequency, high frequency, or a known frequency. You most often need to address high-frequency-noise issues.

You can filter noise using passive analog filters, filter ICs, and digital filters (Figure 2). The most common method, passive filtering, involves creating a passive network of resistors, capacitors, and inductors. You must design passive filters, however, and you cannot easily alter them. Filter design can be as cumbersome as the order of the filter you need; a first-order Chebyshev filter takes much less effort to design than an eighth-order Bessel filter. So you should determine the order of the filter you need before selecting the method of filtering you will employ.

Some ICs allow you to digitally program the type of filter you need. These ICs use internal analog circuitry to create the filter and may have offset voltages associated with them. They also allow you to move the filter process after quantification with the ADC. Digital-filter design can be complex, but many

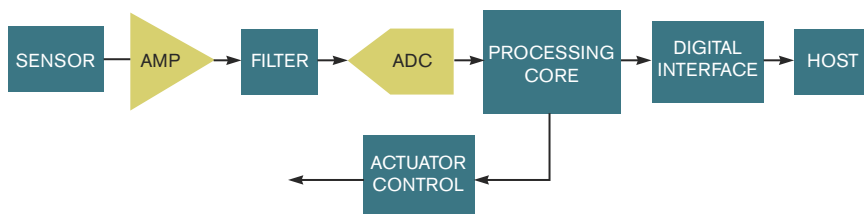


Figure 1 A sensor's analog-signal path goes through several stages: amplification, filtering, and digitization.

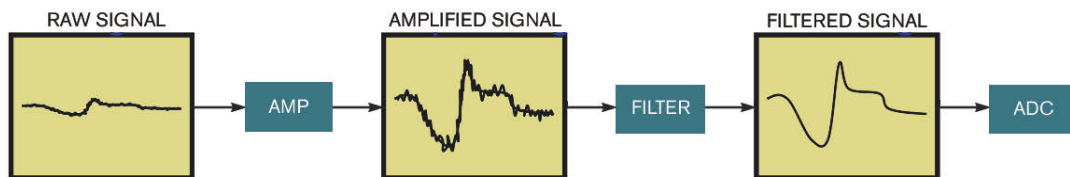


Figure 2 The sensor-signal path includes amplifiers, filters, and an ADC. You design the filter to remove noise and limit the bandwidth of the signal.

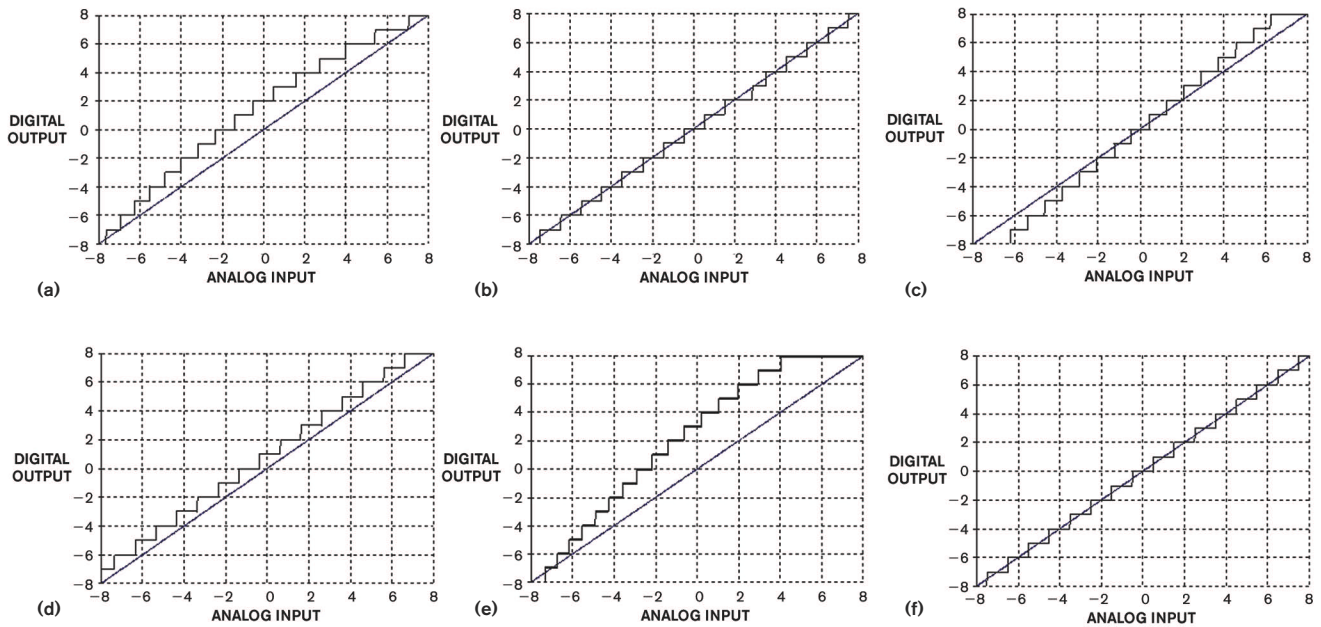


Figure 3 Combining INL error (a), DNL error (b), gain error (c), offset error (d), and total error (e) provides an understanding of the ADC in use compared with an ideal ADC (f).

tools allow for the easy design of high-order filters. Digital filtering can be an ideal means of removing noise; however, it often requires many CPU cycles, increasing power consumption. The system normally incurs high-frequency noise, necessitating the use of a lowpass filter. This filter attenuates any part of the signal that is higher frequency than the set cutoff frequency. Some sensor signals require the use of several types of filters in tandem with each other. Most sensor data sheets specify a basic interface circuit but do not mention the necessary filtering. System designers must create the system before fully

understanding how much filtering is necessary.

### DIGITAL CONVERSION

To use the sensor's filtered signal, you must quantify the analog signal into the digital domain using an ADC. Selection of an ADC mainly concerns the system's requirements for sampling speed and resolution. The necessary sampling speed relates to the sensor's bandwidth or how often the system needs updating. Resolution depends on the granularity you need for the ADC to react to the sensor's information. The system's usage model defines this speed and resolution require-

ment. For example, a generic gyroscope measures  $360^\circ$  of rotation at  $0.67 \text{ mV}/^\circ$ , resulting in an output range of 241 mV. To remain upright, a hobbyist's helicopter might need information from a gyroscope at a granularity of  $1^\circ$  but with a throughput of 10k samples/sec. This requirement would necessitate a 10-bit ADC, which would provide  $0.35^\circ/\text{bit}$ . Note that the signal still has noise on it, however, and  $\pm 1$  bit is acceptable. Conversely, a digital camera with image stabilization might require a granularity of  $0.02^\circ$  but with a throughput of 5k samples/sec to adjust the image sensor as a camera shakes. This requirement would necessitate the use of a 16-bit ADC, which would provide  $0.005^\circ/\text{bit}$ .

Manufacturers measure the accuracy of ADCs in terms of INL (integral nonlinearity), DNL (differential nonlinearity), offset error, gain error, and SNR (signal-to-noise ratio). When you combine these terms, they offer an understanding of the ADC's total error (Figure 3). For most applications, it is not necessary to look into these ADC specifications, but engineers should have a thorough understanding of these values for the ADC in use. You have the choice of using an external ADC or a microcontroller with an integrated ADC.

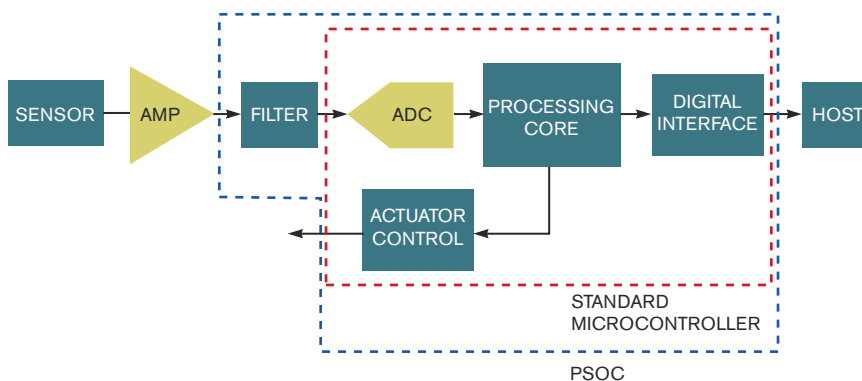


Figure 4 Developers can implement the amplification and filtering stages, integrating the entire analog-signal chain onto one device.





External ADCs tend to have higher accuracy and higher performance in both speed and resolution. Most sensor-application requirements align well with integrated-microcontroller ADCs, however.

Another option is to use configurable ADCs, which comprise programmable logic blocks within a microcontroller. Integrated digital and analog programmable blocks allow for the dynamic definition of configurable peripherals for each sensor application. These blocks include counters, PWMs (pulse-width modulators), UARTs, SPIs (serial-peripheral interfaces), amplifiers, filters, ADCs, and DACs. Developers can also implement the amplification and filtering stages, integrating the entire analog-signal chain onto one device (**Figure 4**). Using configurable ADCs can result in cleaner designs than those using passive components. In addition, you can dynamically reconfigure these blocks, so you have the option of reusing these system resources for other functions.

Sensors continue to penetrate a range of markets, bringing you more control

## SENSORS CONTINUE TO PENETRATE A RANGE OF MARKETS, BRINGING YOU MORE CONTROL AND GREATER FLEXIBILITY.

and greater flexibility. Sensors increase reliability through management of the environment, including, for example, temperature monitoring; improved performance through feedback mechanisms; and enabling new types of user interfaces. For many of these designs, the integrated ADCs on microcontrollers provide sufficient granularity and accuracy. Developers who are unfamiliar with analog design may encounter pitfalls along the analog-signal chain between the sensor and the microprocessor.

Implementing the multiple stages of the analog-signal path can seem convoluted, especially to engineers accustomed to designing primarily in the digi-

tal domain. However, by breaking down the analog-signal path into the various amplification, filtering, and ADC stages, digital-system developers can more easily and accurately capture sensor data for a variety of industrial and consumer applications. In addition, readily available ICs, configurable ADCs, and filter-design tools can greatly simplify sensor design. **EDN**

### AUTHOR'S BIOGRAPHY

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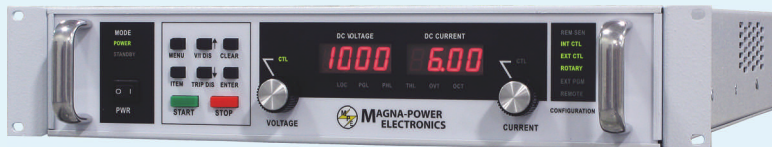


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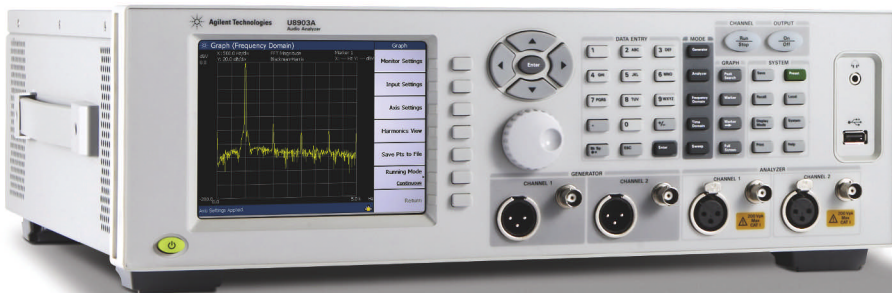
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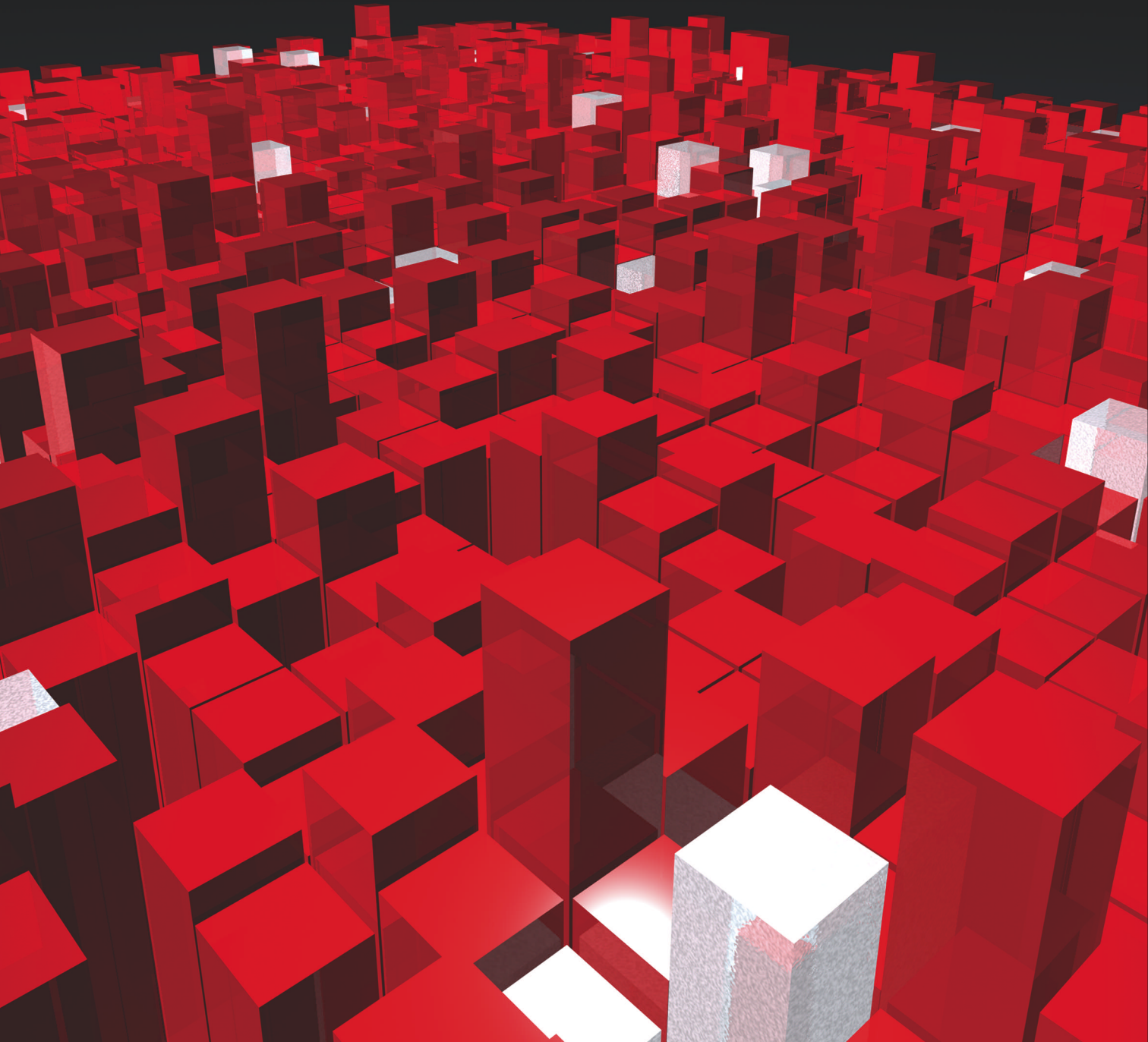


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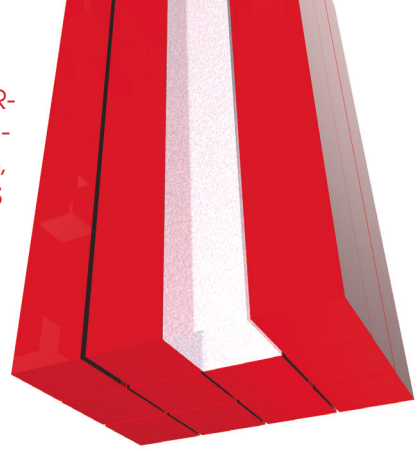
# RF

## SWITCHING OPTIONS: THE RIGHT FIT MIGHT COME WITH A LOSS



MANUFACTURERS ARE OFFERING SOI AND MEMS ALTERNATIVES TO PIN-DIODE, GaAs, AND ELECTROMECHANICAL SWITCHES FOR A VARIETY OF RF APPLICATIONS, BUT YOU NEED TO UNDERSTAND RF-SWITCH SPECS BEFORE YOU COMMIT TO A NEW TECHNOLOGY.

BY RICK NELSON • EDITOR-IN-CHIEF



Whether you are building “big-iron” RF-test equipment or tiny, multiband mobile devices, you need to route RF and microwave signals among instruments and devices under test or between antennas and amplifiers. To accomplish that task, you can turn to various solid-state implementations, including SOI (silicon-on-insulator) devices and MEMS (microelectromechanical-system) switches, both of which vendors were touting at the June IEEE MTT-S (Microwave Theory and Techniques) International Microwave Symposium. Highly integrated bulk-CMOS devices represent another alternative. However,

you need to know when those options make sense as alternatives to the more traditional electromechanical, PIN-diode, and GaAs (gallium-arsenide) FET versions. Solid-state and MEMS switches take up much less real estate and have longer lifetimes than do electromagnetic switches. Further, SOI and MEMS devices can be easier to integrate than GaAs devices with other components. Before embarking on switch selection, however, you need to understand whether the specs of the device you select will meet your application requirements.

### GETTING TO KNOW SPECS

You need to consider switch bandwidth. The switch you choose must, at its maximum operating frequency, conduct a signal. Unfortunately, when choosing a switch, you can't rely on the “3-dB-down”—that is, noise that is 3 dB lower than peak noise—rule of thumb that you might use to determine the upper operating limit of an amplifier, for example. You need to determine the acceptable

performance with respect to bandwidth in the context of the other specifications, including characteristic impedance and VSWR (voltage-standing-wave ratio), crosstalk, and isolation (Reference 1).

You should also consider whether you need to transmit low frequencies or dc. Electromechanical and FET switches generally pass low frequencies; PIN-diode switches and capacitive MEMS switches generally do not (Reference 2).

Other RF-switch specifications include characteristic impedance. You typically use a lumped-element model to represent transmission lines (Figure 1). In these models, successive infinitesimal segments of the line, which ideal transmission lines interconnect, have series resistance  $R$ , series inductance  $L$ , shunt conductance  $G$ , and shunt capacitance  $C$ . Characteristic impedance, then, is

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

For zero resistance and zero conductance, characteristic impedance is

$$Z_0 = \sqrt{\frac{L}{C}}$$

Any switch you select should present the same characteristic impedance your system exhibits to prevent signal reflections. The reflection coefficient quantifies reflections. This coefficient is equivalent to the  $s_{11}$  S parameter (Reference 3), which can contribute to a poor VSWR. With regard to VSWR, you want to know whether you are selecting an absorptive switch or a reflective switch. Absorptive versions apply a resistive shunt to ground in the off state to provide a good impedance match and minimize VSWR, regardless of switch position; reflective versions serve applications in which VSWR doesn't matter or in which you control impedance elsewhere (Reference 4).

### INSERTION LOSS, ISOLATION

Other key specs include isolation, crosstalk, and insertion loss:

$$IL = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

where  $IL$  is insertion loss and  $P_{OUT}$  and  $P_{IN}$  are output power and input power, respectively.

You can also represent insertion loss in terms of S parameters:

$$IL = 10 \log_{10} \left( \frac{s_{21}}{1 - s_{11}} \right)$$

The S-parameter notation to the right of the equal sign shows that the switch's insertion loss is inherent to the switch and does not depend on input mismatches. The  $1 - s_{11}$  denominator indicates that you subtract any reflected



signal that the  $s_{11}$  term represents from the normalized input-signal level before you calculate insertion loss.

Insertion loss is critical, says David Hall, an RF-product manager for National Instruments, which uses RF switches in its lineup of RF-switch-matrix test-and-measurement products. A switch must transmit your signal without undue attenuation at the frequency or frequencies of operation. If you choose a switch with too much insertion loss, he says, you may have to amplify a switched signal to make it usable, adding to system complexity and potentially introducing linearity errors.

## SPECIFYING LINEARITY

A switch can exhibit linearity errors even in the absence of amplification. Specs that indicate linearity include the 1-dB compression point and the IP3 (third-order intercept point). Measuring the 1-dB compression point involves a power sweep on the input to a device under test; when the output drops 1 dB from the level you would expect based on the small-signal response, you've reached the 1-dB compression point. IP3 measurements involve applying closely spaced tones to a nonlinear device under test, which generates third-order intermodulation products. The IP3 point is typically hypothetical because it might lie outside the safe operating region of the device under test. You obtain the IP3 using extrapolation. It occurs when the power of the third-order intermodulation products would equal that of the desired signal (Reference 5).

Other specs include crosstalk and isolation. Crosstalk represents the magnitude of a signal that couples from an active switch to an adjacent inactive switch, and isolation represents the mag-

## AT A GLANCE

▣ You need to determine the acceptable performance with respect to bandwidth in the context of the other specifications, including insertion loss, crosstalk, and isolation.

▣ Absorptive versions apply a resistive shunt to ground in the off state to provide good impedance match and minimize VSWR (voltage-standing-wave ratio) regardless of switch position.

▣ Bulk-CMOS devices offer cost advantages and fit within a small footprint.

▣ One MEMS (microelectromechanical-system) switch is rated for 100 million operations and can work for 1 billion cycles.

▣ The handset market offers high-volume opportunities for nine-throw switches going into pentaband phones.

nitude of a signal that a switch transmits from its input to its output when in the open position. A switch can be subject to various deleterious effects, including impedance mismatch, insertion loss, crosstalk, and isolation (Figure 2).

Electromechanical switches as well as PIN diodes and GaAs FET switches traditionally have excelled at meeting these specs, but each offers drawbacks. Electromechanical switches are large and can occupy significant amounts of PCB (printed-circuit-board) real estate. PIN diodes include a high-resistivity intrinsic region between their P- and N-type semiconductor regions (Reference 6). The intrinsic region becomes conductive when you forward-bias the device, essentially closing the switch to allow RF signals to pass. PIN diodes are rugged, compact devices that can handle

high voltages and currents; drawbacks include the need for external bias circuitry and the fact that the required dc bias current—and the higher the bias, the lower the insertion loss—makes them problematic for use in power-sensitive battery-operated system.

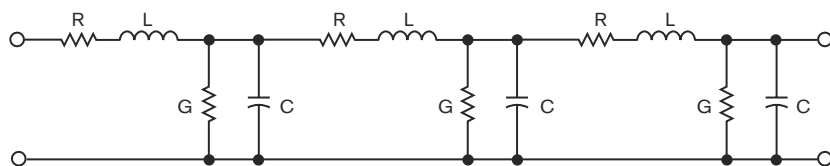
## GaAs DEVICES ARRIVE

GaAs devices remain popular. NEC markets the devices for wireless applications (Reference 7). At the June International Microwave Symposium, RF Micro Devices introduced its 6-GHz RF3021, RF3023, RF3024, and RF3025 switches, which it fabricated in its GaAs PHEMT (pseudomorphic-high-electron-mobility-transistor) technology. The symmetric SPDT (single-pole/double-throw) RF3021 and RF3025 switches feature high isolation; the RF3023 and RF3024 symmetric SPDT switches feature low insertion loss and moderate isolation. This year, Skyworks Solutions Inc introduced its Sky13317-373LF, a PHEMT GaAs SP3T (single-pole/three-throw) antenna switch that operates from 0.1 to 6 GHz. Last month, Hittite Microwave Corp introduced its GaAs PHEMT, MMIC (monolithic-microwave-integrated-circuit), SP4T (single-pole/four-throw), nonreflective HMC-C071 switch module, which targets microwave radio, VSAT (very-small-aperture-terminal), military and aerospace, fiber-optic, and broadband-test applications requiring operation from dc to 20 GHz.

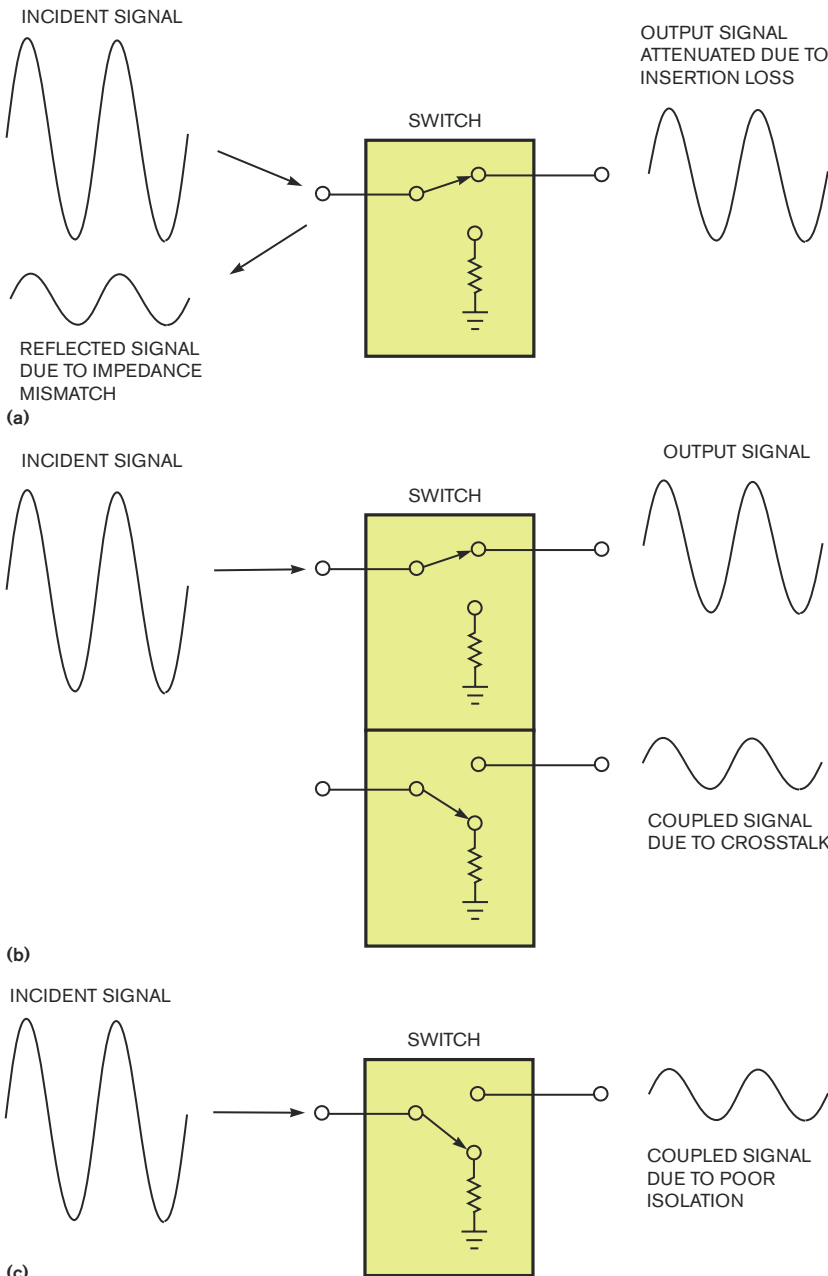
GaAs FET switches have their drawbacks, however, in that they require external components in the form of blocking capacitors, and they can be difficult to integrate with other components (Reference 8). Alternatives to GaAs switches, as well as to electromechanical switches and PIN diodes, include bulk-CMOS, MEMS, and SOI switches.

## BULK-CMOS SWITCHES

Analog Devices touts its ADG9XX-family submicron, 1-GHz bulk-CMOS switches (Figure 3), which the company offers for use in the 900-MHz ISM (industrial/scientific/medical) band (Reference 9). Ray Goggin, staff design engineer, and John Quill, engineering manager, both of Analog Devices' switches-and-multiplexer-product line, cite several advantages of the devices. For exam-



**Figure 1** Lumped-element models typically represent transmission lines, with successive infinitesimal segments, interconnected by an ideal transmission line, having series resistance R, series inductance L, shunt conductance G, and shunt capacitance C, from which you can calculate characteristic impedance. Your switch should offer the same characteristic impedance.

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**Figure 2** A switch can be subject to various deleterious effects. An impedance mismatch can result in input reflections, and the switch's insertion loss attenuates the output signal (a). In addition, an active switch can couple a signal to an adjacent inactive switch (b), and an open switch can couple a signal from its input to its output (c).

ple, they require no dc-blocking capacitors and come in small packages, such as the ADG919's 3×3-mm QFN. They also operate on supply voltages of 1.65 to 2.75V, and they consume less than 1 μA of current. In addition, the devices accept TTL (transistor-transistor-logic) inputs, simplifying their integration with other system components. At 1 GHz, in-

sertion loss is 0.8 dB and isolation is 43 dB. As for power-handling capability, the 1-dB compression point is 17 dBm. The devices successfully pass 1-kV HBM (human-body-model) ESD (electrostatic-discharge) tests on RF pins and 2-kV HBM ESD tests on non-RF pins. The switches are available in absorptive and reflective versions.

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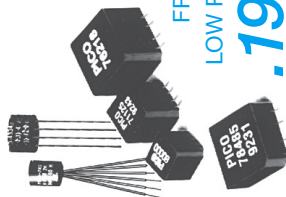
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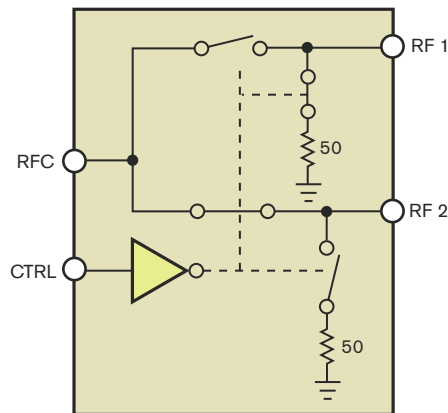
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Goggin and Quill note that bulk-CMOS switches have lower bandwidth and maximum switched-RF power than do other switches, but, for applications whose requirements fall within bulk-CMOS limitations, the bulk-CMOS devices offer cost advantages. They also note that each device exhibits a footprint as small as 9 mm<sup>2</sup> in a CSP (chip-scale package) and can integrate driver circuitry, thereby eliminating the need for separate ICs.



## MEMS AND SOS DEVICES

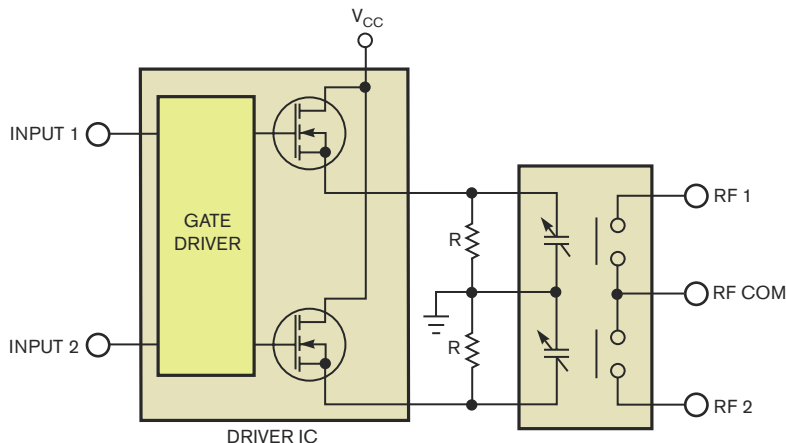
If your application requires performance levels that lie beyond what bulk-CMOS devices can provide, you might consider a MEMS switch. Omron's 2SMES-01, for example, operates to 10 GHz, offering 30-dB isolation and 1-dB insertion loss (Figure 4). It offers maximum power consumption of 10  $\mu$ W, which, according to Donna Sandfox, product manager at Omron Electronic Components LLC, is about one ten-thousandth that of an equivalent electromagnetic relay.

The device targets high-throughput ATE (automated-test-equipment) applications. An electrostatic-drive system powers the device, which performs 100 million operations switching a resistive load at 0.5 mA and 0.5V dc. Sandfox says the company has tested the device over 1 billion cycles. Each switch con-

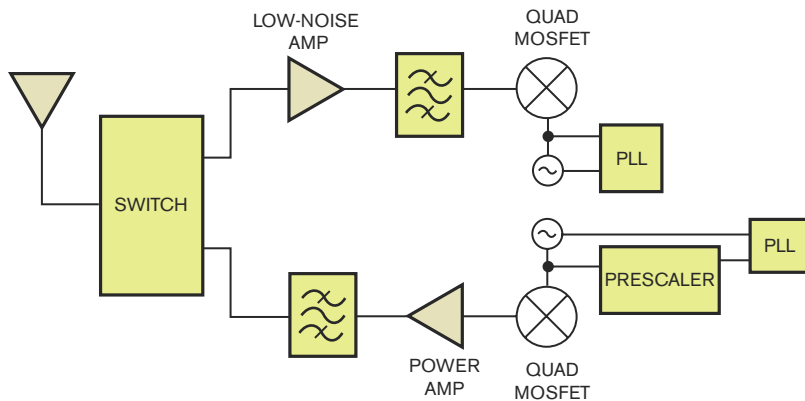
**Figure 3** The Analog Devices SPDT ADG918 absorptive switch has 50 $\Omega$ -terminated shunt resistors to ground, minimizing reflections back to the RF source. It is available in a 3 $\times$ 3-mm chip-scale package.

sists of two normally open SPST (single-pole/single-throw) silicon switches in a 5.2 $\times$ 3.0 $\times$ 1.8-mm housing offering SPDT or DPST (double-pole/single-throw) normally open operation.

Peregrine Semiconductor addresses the RF-switch market with its Ultra-CMOS SOS (silicon-on-sapphire) technology, which integrates ultrathin-silicon-CMOS circuitry on an insulating dielectric sapphire substrate. Peregrine also targets ATE and other applications, including digital TV, cable and satellite set-top boxes, game consoles, and cellular communications. For RF trans-



**Figure 4** An electrostatic-drive system powers Omron's 2SMES-01, which operates to 10 GHz, offering 30-dB isolation and 1-dB insertion loss. It performs 100 million operations switching a resistive load.



**Figure 5** For RF-transceiver applications, Peregrine Semiconductor complements its switches with UltraCMOS quad MOSFETs, PLLs, and prescalers.

ceivers, the company complements its switches with UltraCMOS quad MOSFETs, PLLs, and prescalers (**Figure 5**), enabling Peregrine parts to make up a substantial portion of the RF-signal chain. Rodd Novak, vice president of sales, marketing, and business development, says that the handset market offers high-volume opportunities, with the company's nine-throw switches going into pentaband phones.

For ATE applications, Peregrine offers the PE42552 absorptive SPDT device, which operates to 7.5 GHz with a 1-dB compression point of 34.5 dBm. Insertion loss is 0.65 dB at 3 GHz. Also for ATE applications, the company complements the PE42552 switch with the PE43703 7-bit digital step attenuator.

Mark Schrepferman, director of sales and marketing for communications and industrial markets at Peregrine, says that Peregrine has learned a lot about how to serve the test-equipment market from looking at its own test needs. Christian Steele, product-development section manager at Peregrine, recounts one major problem. Big-box ATE systems, he says, often include one or two sources and one or two receivers and rely on electromechanical switches to route signals among the available instruments and the multiport devices under test. "A lot of those mechanical switches have a reliability of very few throws—often less than 2 million," he explains. "At the volumes in which we are shipping our handset switches, we would be replacing very expensive mechanical switches in

less than a month." The cover story of the October issue of EDN's sister publication *Test & Measurement World* will describe how Peregrine engineers perform engineering characterization and production test of SOS devices.

Schrepferman says he has learned a lot from Steele and colleagues involved in test at Peregrine and has put the infor-

mation to good use. He notes that, even in the down economy, the company has seen "a tremendous number of design wins" in the test-equipment market.

As RF-switch technology advances, there is unlikely to be a clear-cut winner serving all applications, and Peregrine is evaluating multiple technologies. At Peregrine, there is one restriction. Ron Reedy, co-founder and chief technology officer, says that he put one edict in place when he founded the company: "Don't get in front of the CMOS steamroller." If you can implement something in bulk silicon CMOS, which he calls mankind's greatest volume accomplishment by any standard, then that's how you should implement it.

Reedy says that Peregrine is investigating MEMS, noting that, "from a performance point of view, it's pretty hard to beat metal contact." It's counterproductive, however, to put a high-performance switch on a lossy substrate, and work is under way to see whether MEMS belong on sapphire. "We would not say there is a single technical solution that covers all applications," he adds. **EDN**

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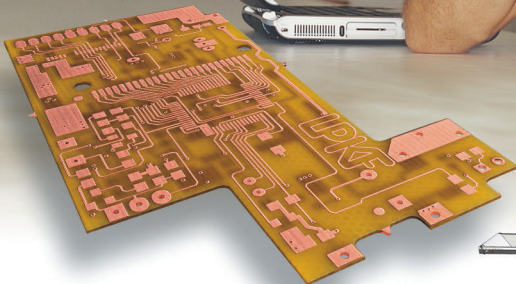
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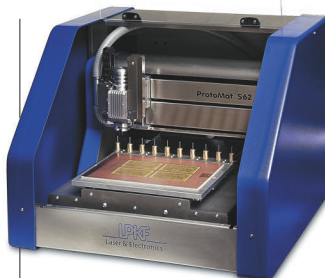
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



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					typ.	max.	typ.	max.			
RJK03C0DPA	30	+20/-20V	70	65	1.8	2.5	1.5	2.0	13.7	66	0.75
RJK0390DPA			65	60	2.1	2.9	1.7	2.2	11.3	54	0.8
RJK0391DPA			50	50	2.8	3.9	2.2	2.9	7.4	34	0.95
RJK0392DPA			45	45	3.4	4.8	2.7	3.5	5.9	26	0.8
RJK0393DPA			40	40	4.2	5.9	3.3	4.3	4.7	21	1.4
RJK0394DPA			35	35	5.3	7.4	4.1	5.3	3.7	15.5	1.4
RJK0395DPA			30	30	7.6	10.6	5.9	7.7	2.6	11.0	2.2
RJK0396DPA			30	28	9.0	12.6	6.9	9.0	2.2	9	2.5
RJK0397DPA			30	25	10.4	14.6	7.8	10.1	1.9	7.4	2.5
RJK03B7DPA			30	30	7.7	10.7	6.0	7.8	2.6	11.0	1.0
RJK03B8DPA			30	28	9.3	12.9	7.0	9.3	2.2	9	1.2
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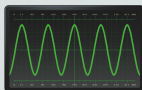
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# In search of a better DRAM: evolving to floating bodies

**WIDELY INVESTIGATED FLOATING-BODY MEMORIES APPEAR TO BE COMPELLING REPLACEMENTS FOR CONVENTIONAL DRAMs. A NEW FLOATING-BODY MEMORY USES THE INTRINSIC BIPOLAR TRANSISTOR TO STORE SIGNIFICANTLY GREATER CHARGE.**

The memory industry has crammed more and more memory bits onto ever smaller die and is selling those slivers of silicon for a few cents each. Currently, 1-Gbit and even 4-Gbit DRAMs (dynamic random-access memories) are available. Process engineers have been able to achieve these goals, especially with respect to the capacitor element, which has become more difficult to scale, a problem that gets worse as device geometries shrink. These advances employ the basic one-transistor DRAM, which Robert H Dennard, PhD, a fellow at the IBM Thomas J Watson Research Center ([www.watson.ibm.com](http://www.watson.ibm.com)), created in 1966. In 1970, Intel ([www.intel.com](http://www.intel.com)) released the first DRAM chip, a 1-kbit PMOS device. Since that time, the basic DRAM building block has comprised a single transistor and an increasingly complex capacitor.

Scaling introduces yet another major problem for DRAM manufacturers: leakage current. In both the bit cell and its supporting circuitry, leakage becomes more significant as CMOS (complementary metal-oxide-semiconductor) processing nodes progress from 90 nm through 78, 50, and 45 nm. Manufacturers are now discussing building memory chips at the 32-nm node. At this point, leakage in traditional designs will become a difficult problem and prohibitively expensive to counteract, requiring new architectures, changes to standard operating specifications, and significant process evolutions.

The problems of scaling and leakage, as well as device size, rest fundamentally with the basic transistor-plus-capacitor

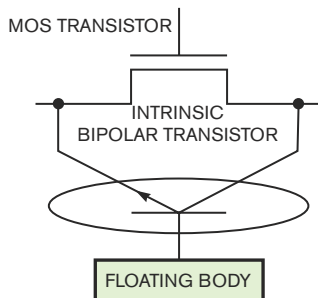


Figure 1 The use of an intrinsic bipolar transistor results in a superior floating-body-memory design.

building block. Although the transistor element is theoretically infinitely scalable, at least for the foreseeable future, the capacitor is not. Manufacturers can fabricate capacitors as either high stacks or deep trenches. However, if the overall bit cell shrinks due to increased density or a smaller process node, the capacitor must become higher or deeper to maintain the minimum charge necessary for reliable operation.

The memory industry is fast approaching the scaling limits for the capacitor element, and it is therefore time for a new approach. There appears to be a groundswell of opinion in the commercial world and the analyst community that floating-body-based

memories may provide the answer. The floating-body effect is the dependence of the body potential of a transistor, using the SOI (silicon-on-insulator) technology, on the history of its biasing and the carrier-recombination processes. The transistor's body forms a capacitor against the insulated substrate. The charge accumulates on this capacitor and may cause adverse effects—for example, opening parasitic transistors in the structure and causing off-state leakages, resulting in higher current consumption and, in DRAM, the loss of information from the memory cells.

Multiple significant companies, notably Samsung ([www.samsung.com](http://www.samsung.com)), Intel, and STMicroelectronics ([www.st.com](http://www.st.com)), have published work on the subject, and at least three pa-

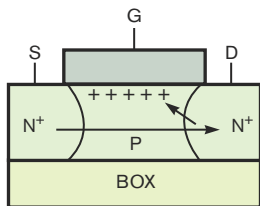


Figure 2 The write cycle for a one data pattern generates current flow through the transistor body.

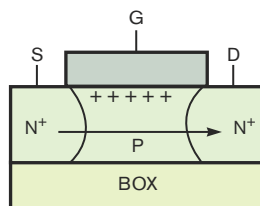


Figure 3 A read-cycle mechanism senses bipolar current flow.

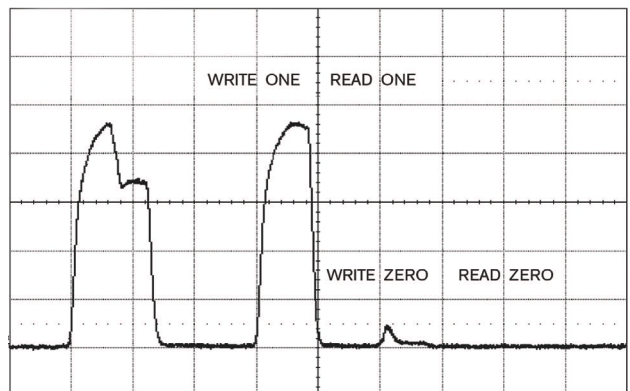


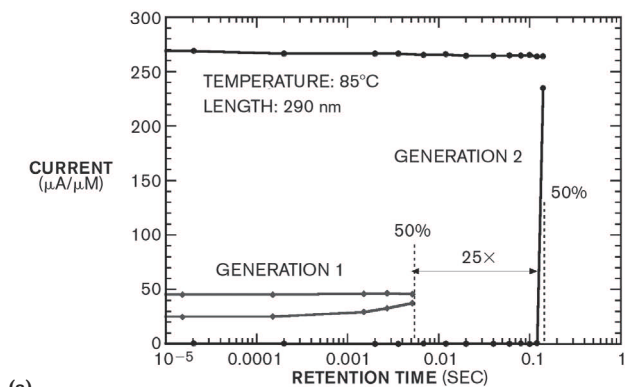
Figure 4 Read and write currents are nearly identical.

pers presented at the International Electron Devices Meeting, which took place in December 2008 in San Francisco, addressed floating bodies. Equally significant, at least one major stand-alone-memory maker, Hynix ([www.hynix.com](http://www.hynix.com)), and one processor company, AMD ([www.amd.com](http://www.amd.com)), have signed

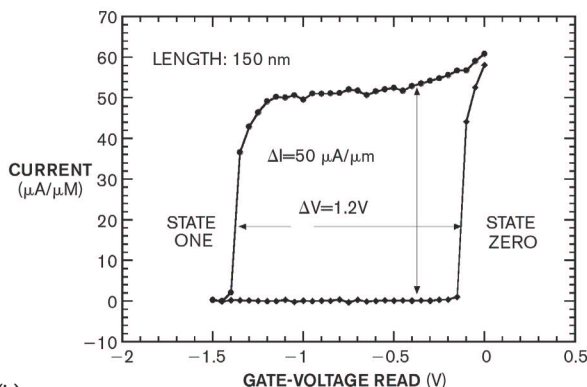
licenses with a floating-body-memory company to develop products.

The floating-body effect naturally occurs in transistors fabricated on SOI substrates, leading to the accumulation of charge in the transistor body. Recently introduced device types such as FinFETs (fin-shaped field-effect transistors) and surround-gate, or pillar, transistors also demonstrate a floating-body effect, even when you implement them on traditional bulk-CMOS substrates. For these reasons, engineers no longer regard the floating-body effect as a parasitic nuisance. Many engineers have tried to manipulate and enhance the body charge so that they can use it to reliably store a logical “state” and function as a memory element. The objective is a memory bit cell that comprises only one transistor, fundamentally the simplest and most scalable of all semiconductor devices.

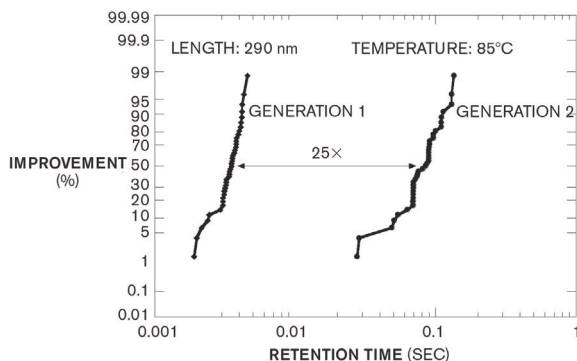
Although a number of companies have investigated floating-body memories, the conventional approach is unlikely to lead to a manufacturable product. A second generation of floating-body memory must be able to store a significantly larger charge in a smaller transistor. This increased amount of charge greatly improves the amount of time the memory can retain its state as well as the signal margin between a one state and a zero state. Other improvements include faster reads and writes and reduced write power consumption.



(a)



(b)

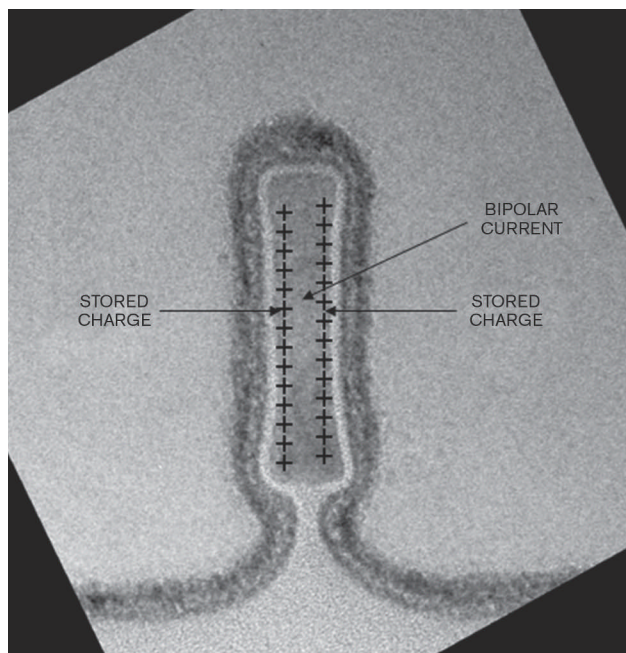


(c)

**Figure 5** A retention-measurement comparison of first-generation (MOS-transistor element only) and second-generation (added bipolar element) floating-body memories reveals the second generation’s superiority (a). The bipolar-inclusive floating-body approach also delivers a more substantial programming window (b), along with a 25-fold improvement in retention time (c).

## PRINCIPLES OF OPERATION

Early attempts at realizing usable floating-body memories employed a MOS transistor to pass current and create charge in the body using impact ionization. Although you can demonstrate memory performance using such a technique, the amount of charge you create with this method is insufficient to create a robust and manufacturable memory device. A superior approach is to use the bipolar transistor intrinsic in



**Figure 6** A FinFET design is amenable to floating-body techniques.



the SOI-MOS structure to create charge (Figure 1). This approach allows the creation of a much larger charge and the ability to store more charge because of the increased capacitance of the memory cell.

If you consider an N-channel device, the N+ source, the P-type body, and the N+ drain form the emitter, base, and collector, respectively, of an NPN (negative-positive-negative) bipolar transistor. The body of the MOS transistor is the base of the bipolar transistor and acts as a storage node. Writing a one into a second-generation bipolar floating-body-memory cell triggers the intrinsic bipolar transistor, causing current to flow throughout the transistor body. This approach differs significantly from the behavior of MOS, in which current flows only at the interface. Charge collects at the interface due to the slight bias at the gate. The impact-ionization effect that creates an excess of majority carriers in the floating body is more efficient in this bipolar bit-cell structure, quickly charging the body and therefore resulting in rapid writes (Figure 2).

You can read a floating-body memory using a similar mechanism, which senses the bipolar current through the transistor (Figure 3). Write current is close in value to the read current, and the latch-up characteristic of the intrinsic bipolar quality causes the behavior of the memory cell to appear nearly digital (Figure 4).

#### CELL MARGIN AND SCALABILITY

Bipolar floating-body memories have a significantly higher operating margin than traditional floating-body devices, al-

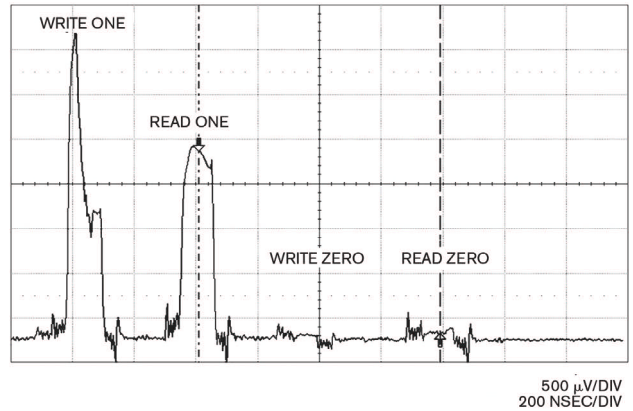


Figure 7 The read and write currents for a FinFET with a length of 55 nm and width of 11 nm reveal its robust capabilities.

lowing them to create faster memory bit cells. The operating margin is better for two reasons: The storage charge is higher, and the difference between the one and the zero states is much larger because the bipolar element is a better amplifier than a MOS device (Figure 5). A high cell margin eases sensing using a simple sensing scheme. The approach also simplifies the sense amplifier's design. When you implement floating-body memories with conventional planar transistors, the memories'

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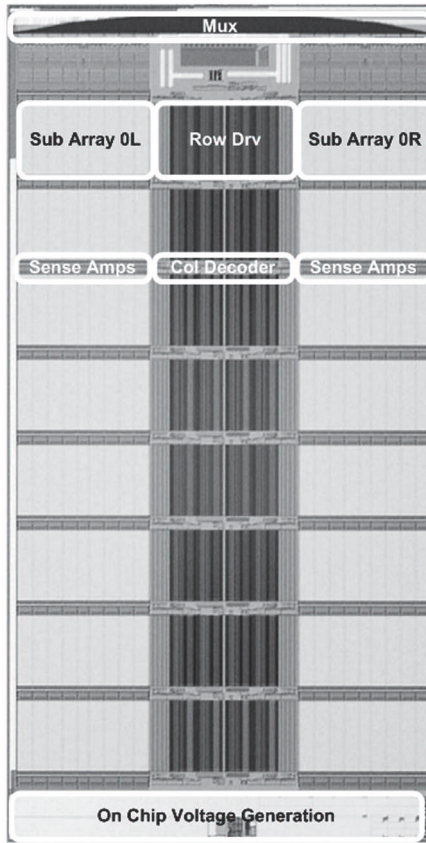
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large voltage margin helps to mitigate the negative effects of process fluctuations, which become increasingly significant at smaller process geometries. Perhaps just as important, the new bipolar floating-body-memory designs are compatible with advanced, nonplanar devices, such as FinFET, multigate FET, and gate-all-around FET. Older floating-body designs work on only thin-film planar devices.

### FINFETs AND ARRAYS

FinFETs, surround-gate transistors, and other similar 3-D structures should provide the basis for future stand-alone memories as the industry scales to ever smaller process geometries. Working at the 54-nm node, some DRAM companies are using FinFET designs, and most suppliers should follow in the next five years. Manufacturers can fabricate FinFETs and pillar transistors on both SOI and conventional bulk substrates. In a FinFET or trigate-based Z-RAM (zero-capacitor RAM), the



TECHNOLOGY	45-NM PARTIALLY DEPLETED SOI
MEMORY TRANSISTOR	WIDTH: 112 NM, LENGTH: 112 NM, OXIDE THICKNESS: 3 NM
CELL SIZE	0.480×0.192 MICRONS (0.0922 MICRONS <sup>2</sup> )
MACRO SIZE	1323×718 MICRONS (FOR 4.44 MBITS)
DENSITY	0.21 mm <sup>2</sup> /MBIT
SUBARRAY	LOCAL SENSING WITH 260 ROWS/BIT LINE AND 1120 BITS/ROW
REDUNDANCY	FOUR ROWS AND 16 COLUMNS PER SUBARRAY
ECC	9 ECC CHECK BITS PER WORD
SENSING	VOLTAGE, EIGHT-BIT-LINE PITCH, CORE TRANSISTORS
ROW DRIVERS	FOUR-WORD-LINE PITCH, WORD-LINE DRIVERS WITH BT DUAL-GATE OXIDE DEVICES
INTERFACE	140-BIT DATA WORD, 15-BIT ADDRESS, 7-BIT CONTROL
PERFORMANCE	4-NSEC RANDOM ACCESS, 2-NSEC* READ LATENCY, 2-GHz CYCLE TIME

\*WORD LINE HIGH TO SENSE AMPLIFIER'S OUT TIME

Figure 8 You can implement a 4-Mbit macro in a 45-nm SOI process.



Noises removed by Samsung capacitor

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(0402 X5R 2.2uF 6.3V, 0402 X6S 0.47uF 4V)

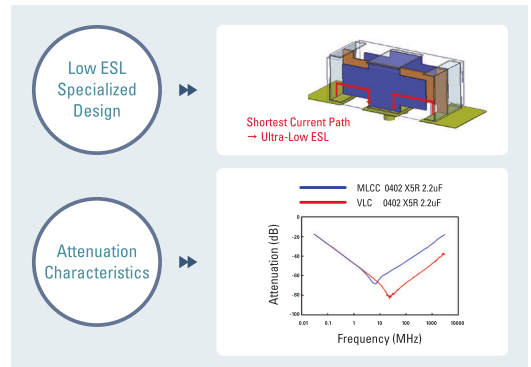
VLC(Vertically Laminated Capacitor) has vertically oriented internal electrodes that effectively reduce the current loop area in the device. Therefore, it provides ultra-low equivalent series inductance (ESL) despite its relatively simple terminal structure. This innovative capacitor is recommended for various package applications(CPU, GPU), mobile phone, and laptop, etc.

### FEATURES

- Ultra Low ESL
- Rated Voltage 6.3 or 4Vdc
- X5R or X6S TCC

### ADVANTAGES

- Excellent Bypassing Characteristic
- Saving Space by Replacing 4 MLCC's
- No Tomb-stoning





charge accumulates under the transistor gate, and the current flows in the middle of the fin structure. The fin stores charge throughout the structure, permitting excellent control of the bipolar current (Figure 6). Bipolar floating-body-memory implementations using FinFET structures tend to exhibit an approximately 30-fold increase in margin, leading to a proportional increase in signal and device speed. Figure 7 shows the cell current during write and read. Even an undoped cell with an 11-nm fin shows clean digital behavior and a good margin. Floating-body memory continues to scale with technology whether you fabricate on planar or 3-D structures.

For the successful implementation of floating-body memories, it is crucial to create memory-bit-cell arrays. Original floating-body implementations, due to the limited possible margin between the one and the zero states, are relatively slow and therefore unsuitable for combining into useful arrays. However, new bipolar floating-body-memory cells, which produce superior signal margins due to the large current gain available from the bipolar device, enable more robust arrays (Figure 8).

The macro for these memories supports a 2-nsec read latency and a 4-nsec write latency. It also implements a high-speed page mode to read a 140-bit word during every 2-GHz-processor clock cycle, using a shared-I/O bus and data latches at the interface. This macro supports consecutive memory operations at 4 nsec and a burst of four words during page mode. The 4-Mbit memory macro comprises 16 subarrays of 256×1024-bit,

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or 256-kbit, cells (Figure 8). The exact implementation, 260×1120 bits, includes redundancy and ECC (error-correcting code). Subarrays share two banks of sense amplifiers at each end of every subarray and each bank with adjacent subarrays. A combination of column and row operations allows the access of four 140-bit words by simultaneously activating two subarrays on the right and left sides of a shared block of row drivers.

A subset of combined read- and write-restore operations constitutes a refresh operation. A control block outside the 4-Mbit macro initiates refresh. A low-power refresh mode minimizes the voltage swings on inactive bit lines between the read- and write-restore operations of the refresh cycle. The memory macro has a refresh cycle of 1 msec at 105°C, along with three external power supplies of 1.1, 2.6, and 0.5V. A dedicated on-chip voltage-generation block attaches to the memory macro and supplies the required operational voltages. **EDN**

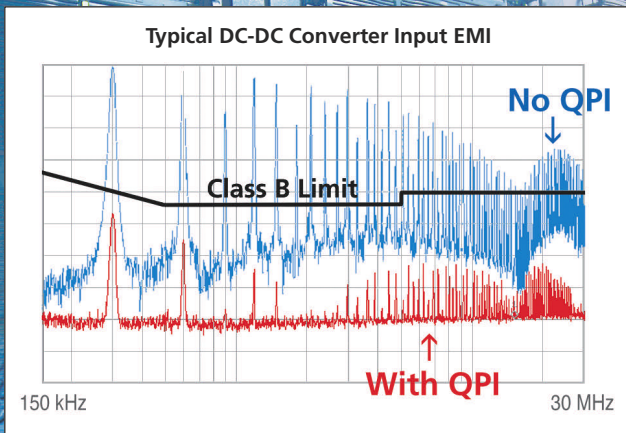
#### AUTHOR'S BIOGRAPHY



Serguei Okhonin, PhD, is co-founder and chief scientist of Innovative Silicon, where he has worked for six years. He has a master's degree in physics from Novosibirsk State University (Novosibirsk, Russia) and a doctorate from the Swiss Federal Institute of Technology (Zurich, Switzerland). His personal interests include skiing, rock climbing, and mountaineering. You can reach him at [sokhonin@z-ram.com](mailto:sokhonin@z-ram.com).

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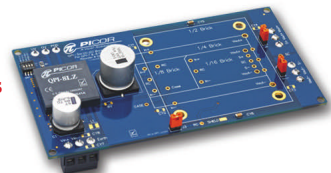
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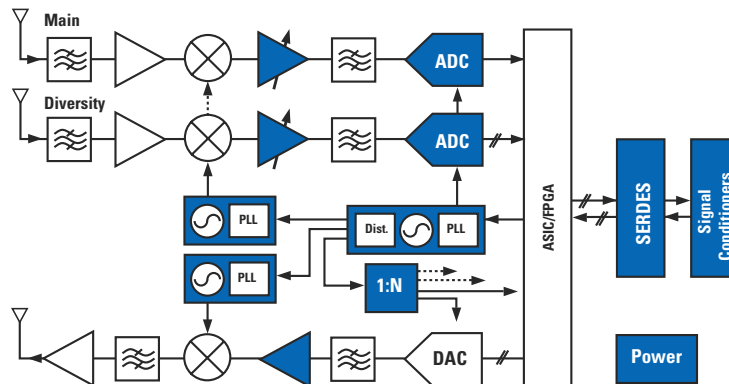


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- ✓ Reference designs
- ✓ Online design tools



Shown: Wireless Basestation Application Diagram

### Low Noise, Low Power

In high-performance basestation designs, linearity and low-noise operation are key to maximizing receiver sensitivity. National's LMH6517 DVGA, combined with the ADC16V130 16-bit ADC, LMK04000 clock jitter cleaner, and LMX2541 frequency synthesizer optimize next-generation multi-carrier GSM, LTE, UMTS, and WiMax base stations.

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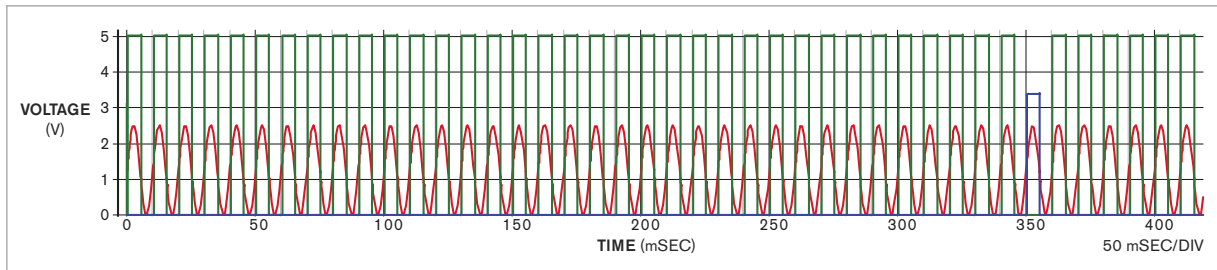
High-power density and efficiency are critical to reduce total power consumption, minimize heat generated by power losses, and improve system reliability and safety. National's diverse portfolio of LM5000 power management solutions maximize power density and end-to-end power chain efficiency.

### Design Flexibility

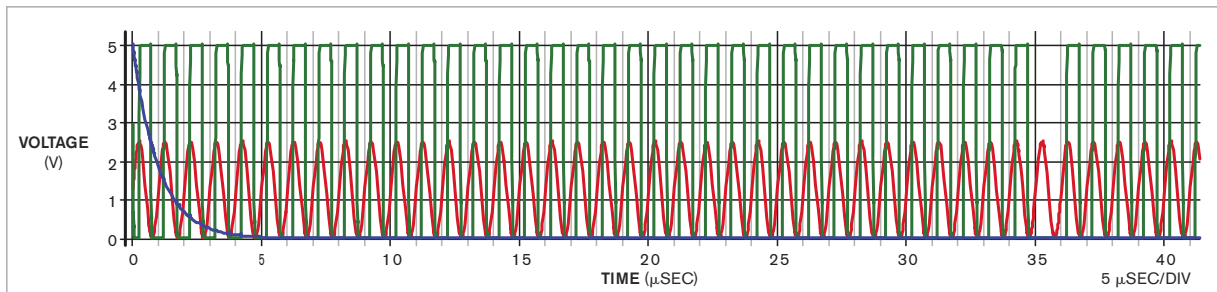
National's DS64BR401 quad 6.4 Gbps transceivers perform signal conditioning on both input (EQ) and output (De-Emphasis) stages to maximize basestation design flexibility and recover from transmission losses induced by backplane or cable interconnects.

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**Figure 2** Operating at 100 Hz, the circuit signals include the clock-sine-wave signal (red), the sense-square-wave signal (green), and the detect signal (blue), which indicates the missing pulse.



**Figure 3** The pulse train at a clock frequency of 1 MHz still shows the missing 36th pulse along with the power-reset signal (blue).

$IC_{3A}$  low. That action puts the D flip-flop into a known state. As  $C_1$  charges through  $R_1$ , the voltage at the power reset falls, letting clock pulses set  $IC_{3A}$ 's outputs. You must keep the small value for the  $C_1/R_1$  combination if you use a high input frequency with a low count rate. As **Figure 3** shows, the desired count must exceed the duration of the power reset. The values in **Figure 1** provide a time of approximately  $0.66 \times 1 \text{ k}\Omega$  (the value of  $R_1$ )  $\times 1 \text{ nF}$  (the value of  $C_1$ ), or  $0.66 \text{ }\mu\text{sec}$ , leaving a minimum count of approximately three at 1 MHz.

For the clock signal, the circuit uses a sine-wave signal with an amplitude of 5 to 10V from the system. The clock signal goes through  $R_3$  to  $D_4$  and  $IC_{1A}$  to produce a 5V square-wave signal. The signal goes to counter  $IC_2$ , and to one input of AND gate  $IC_{4B}$ . With the other input of  $IC_{4B}$  coming from  $IC_{3A}$ 's QN output, which is high from power reset at start-up, the input-pulse train passes through  $IC_{4B}$ , which simulates sprocket teeth at the sensor. Resistors  $R_6$  and  $R_7$  halve the clock-signal amplitude just to make the graphics clear at "signal

in." Diodes  $D_1$ ,  $D_2$ , and  $D_3$  pull up to 5V through  $R_2$  and form an AND gate to select the desired count. Counter  $IC_2$ 's outputs are binary, so, for a 36-tooth sprocket with one missing tooth, outputs Q0, Q1, and Q5 correspond to  $1+2+32=35$ .

You can produce any count as high as 128 by adding the appropriate diodes on the Q outputs on  $IC_2$ . In other words, you need to generate one missing pulse of 36 to simulate the 36-tooth sprocket. Thus, you select a count of 35; the circuit automatically adds a count of one due to the one-clock delay of the counter. Because you reset  $IC_2$  at power-up, all outputs are low, keeping the D input of  $IC_{3A}$  low, with a count of zero.

## THE CIRCUIT AUTOMATICALLY ADDS A COUNT OF ONE DUE TO THE ONE-CLOCK DELAY OF THE COUNTER.


As clock pulses continue into  $IC_2$  and when outputs Q0, Q1, and Q5 are all high, with a count of 35,  $IC_{3A}$ 's D pin pulls high through  $R_2$ . On the next clock pulse, the Q output of  $IC_{3A}$  goes high and the QN output goes low, stopping the pulses from passing through  $IC_{4B}$ . This action indicates the missing tooth and produces the sense condition (the missing pulses in **figures 2** and **3**). Meanwhile, the Q output of  $IC_{3A}$ 's output goes high, yielding a single detect pulse at  $IC_{4C}$  through  $R_4$  and  $R_5$ . On the next clock pulse, with  $IC_{3A}$ 's Q output high,  $IC_2$  resets logic zero and is ready for the next count cycle.  $R_4$  and  $R_5$  halve the clock signal just to make the graphics clear at "detect."

The 4024 is an eight-stage binary-ripple counter. You can replace it with a 4040 counter to achieve a count of 2048, and you can cascade counters to get longer counts or delays. The 4040's pinout differs from that of the 4024, but their operation is identical. Some systems have an extra tooth instead of a missing tooth, and some have multiple missing teeth at odd locations around the sprocket, all waiting for replacement by this simple circuit. **EDN**



# Emulate SPI signals with a digital-I/O card

Andy Street, Autoliv Electronics, Lowell, MA

 A design-verification tester for millimeter-wave SOC (system-on-chip) devices needed to combine switching, electrical measurements, temperature measurement, a parallel-digital interface, and a serial-digital interface into one instrument. To minimize rack space, the circuit uses an Agilent Technologies ([www.agilent.com](http://www.agilent.com)) 34980A multifunction mainframe because its plug-in cards could support a force/sense dc matrix and multiplexed temperature measurements. The addition of an Agilent 34950A 64-bit digital-I/O card formed the basis of a system that could provide both an SPI (serial-peripheral-interface) bus and a simple parallel bus. The 34950A groups its I/O lines into two banks of four 8-bit channels. It provides 64 kbytes of memory per bank for pattern generation or signal capture. It also has three I/O lines per bank for handshaking.

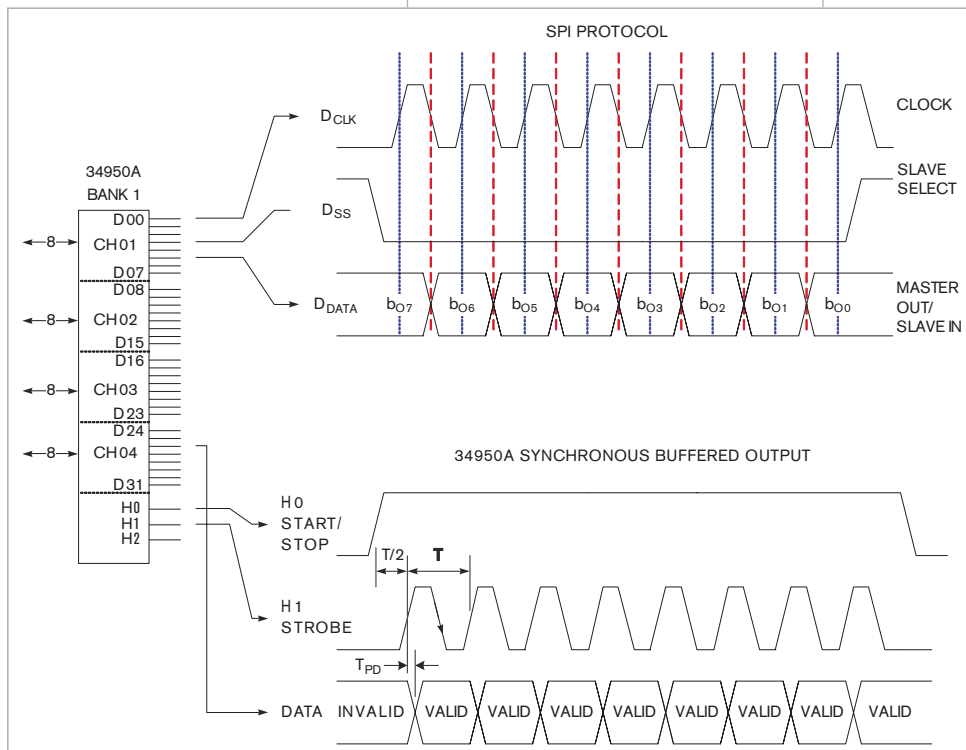
## YOU CAN STORE A MAXIMUM OF 32 TRACES IN THE PATTERN RAM PER BANK.

However, the card's handshake lines provide insufficient control for implementing SPI transactions. To get adequate control, you can emulate the SPI bus using three of the data-I/O lines.

Motorola ([www.motorola.com](http://www.motorola.com)) microcontrollers first used the SPI master-slave protocol. Today, it's become the control interface in a variety of ICs, including PLLs (phase-locked loops) and RF ASICs (references 1 and 2). The SPI bus uses the clock, SS (slave-select), MOSI (master-out/slave-in), and MISO (master-

in/slave-out) lines. The clock line is a signal from the master to the slave. All SPI signals are synchronous with this clock. The SS line selects the slave for communication. The SPI specification defines four modes of operation, which effectively specify the clock edges for toggling and sampling and the clock-idle level. The specification makes no requirements on voltage levels or data rates, and many SPI implementations can clock in excess of 10 MHz. **Figure 1** shows a block and timing diagram of the 34950A's Bank 1, configured for synchronous, buffered output. H0 through H2 denote the handshake lines. The **figure** also shows an 8-bit SPI transaction for reference.

You cannot use the 34950A's handshake lines to emulate all modes of the SPI bus because the bus latches data on the falling edge of the clock, making the bus unsuitable for slaves that use the rising edge. Inverting the clock polarity is not a solution because you may lose the last data bit. Furthermore, if you write a number of transactions to a slave, you must store each transaction as a separate trace memory in the 34950A. Although each bank supports 64k×8 bits, you can store a maximum of 32 traces in the pattern RAM per bank, thereby limiting the number of SPI transactions. In addition, the card lacks a sequencer, so you cannot download a number of bit patterns and then play them in sequence. You must load each pattern into the I/O card's memory and then play each pattern under SCPI (standard commands for programmable instruments) from a host computer, slowing transactions.



**Figure 1** The 34950A synchronous buffered output uses the falling edge, making it unsuited to rising-edge SPI implementations.

Instead of using the handshake lines, this solution uses three da-

ta-I/O lines to emulate the SPI clock, SS, and MOSI. The software driver for the I/O cards then has the responsibility of translating the data to be sent into an SPI-compatible bit stream. **Listing 1**, which is available at [www.edn.com/090917dia](http://www.edn.com/090917dia), contains the algo-

rithm in pseudocode, which translates a hexadecimal string, DH, of characters to an SPI signal. LD, LSS, and LCLK are integers to define which data outputs represent the MOSI, CLK, and SS, respectively.

Assuming a 24-bit register write

with two bits of overhead for the SS prefix and postfix, the 64-kbyte memory can support more than 1000 SPI transactions. The approach has two additional advantages: The three lines that form the SPI bus are under software control, which provides cabling flexibility, and the implementation can support multiple slaves through the use of additional SS lines. **Figure 2** shows an MSO (mixed-signal-oscilloscope) screen that shows the SPI transaction. The SPI clock rate is 5 MHz, which the 34950A's internal 10-MHz clock limits. The different payload sizes correspond to writing data to 16- and 24-bit registers within the slave. **EDN**

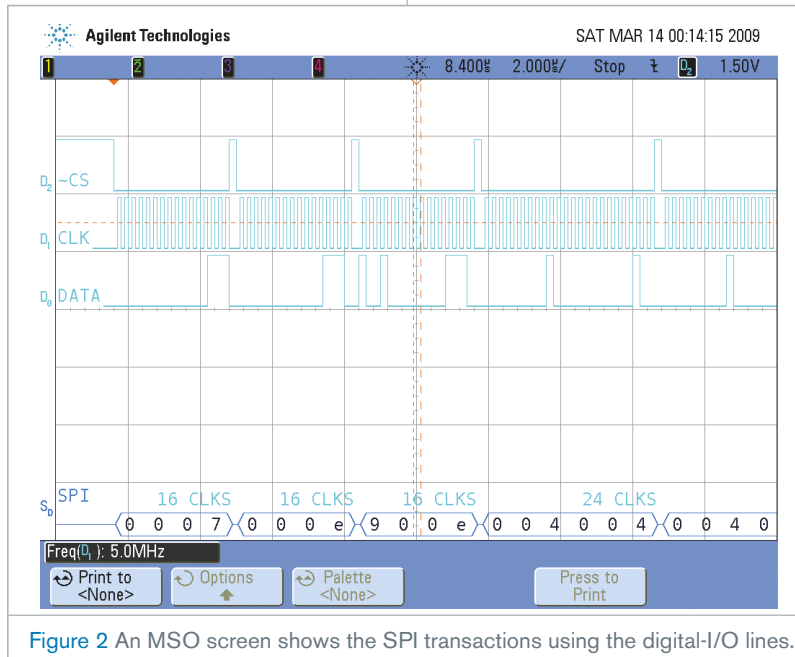


Figure 2 An MSO screen shows the SPI transactions using the digital-I/O lines.

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- "SPI Block Guide V04.01," Freescale Semiconductor, July 2004, [www.freescale.com/files/microcontrollers/doc/ref\\_manual/S12SPIV4.pdf](http://www.freescale.com/files/microcontrollers/doc/ref_manual/S12SPIV4.pdf).

## Resistive DAC and op amp form hybrid divider

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

**A** resistive DAC in a resistive-feedback loop of an op amp lets you create an analog-digital-analog divider. The resistance,  $R_{WA}$ , between the W and A terminals of the Analog Devices ([www.analog.com](http://www.analog.com)) AD5293 (**Figure 1**) decreases linearly with increasing the digital-control data, D:

$$R_{WA}(D) = \frac{1024-D}{1024} \times R_{AB},$$

and the value of the  $R_{WB}$ , the resistance between the W and B terminals of the DAC, rises proportionally to D as

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB}.$$

$R_{AB}$  is a constant value of resistance be-

tween the ends of the digital potentiometer. The circuit uses resistance  $R_{WA}$  as a feedback resistor, and resistance  $R_{WB}$  connects between the inverting input of the op amp and ground. The voltage gain of the noninverting amplifier becomes

$$A_V = 1 + \frac{R_{WA}}{R_{WB}} = \frac{1024}{D}.$$

The output voltage is

$$V_{OUT} = V_{IN} \times \frac{1024}{D}.$$

Both the input voltage and the digital-input data can be time variables, and the clock frequency for fetching digital-input data can be as high as 50 MHz.

The potentiometer's data sheet provides the ground-referred parasitic capacitances at the A, B, and W terminals of the potentiometer. Thorough measurement of the capacitances at these terminals provides enough data to determine capacitances between the terminals. An evaluation of the measured data shows that the direct capacitance between the A and W terminals at the midscale position of the wiper is just 2.4 pF:

$$C_{AW}(X = 1/2) = 2.4 \text{ pF}.$$

If you assume that the five segments of the potentiometer are ordered topologically into a chain, then the direct intercapacitance between the A and B ends of potentiometer is

$$C_{AB}(X = 1/2) = 1/2 C_{AW}(X = 1/2) = 1.2 \text{ pF}.$$

The capacitance per segment of the five segments of the potentiometer is

$$C_{SEGM} \approx 5C_{AB}(X = 1/2) \approx 6 \text{ pF},$$

where  $X=1/2$  denotes the midscale of the resistive DAC.

The five-step distributed RC line of the potentiometer has a time constant of

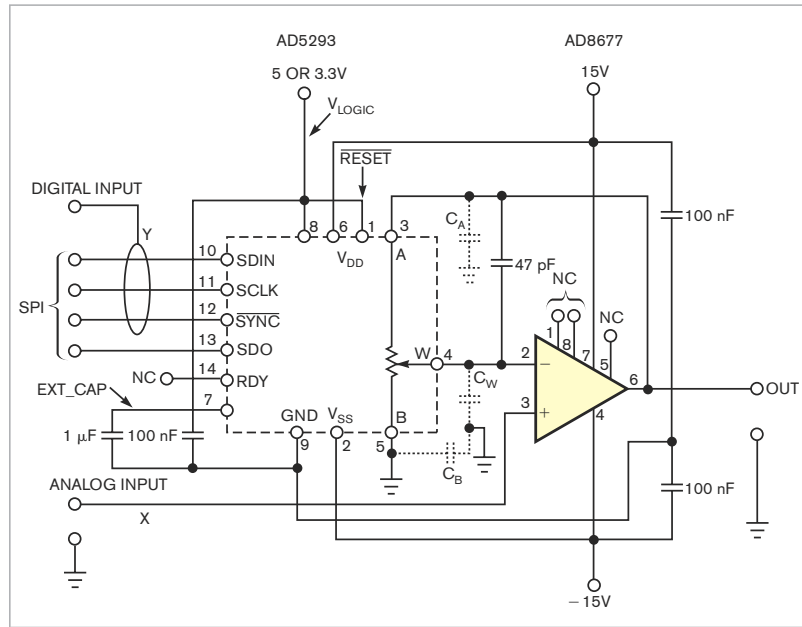
$$\tau_{SEGM} = \frac{R_{AB}}{5} \times C_{SEGM} = R_{AB} \times C_{AB} = 24 \text{ nSEC},$$

where  $R_{AB}$  is 20 k $\Omega$ . The ground-referred wiper capacitance,  $C_W$ , of 40 pF is much higher than the intercapacitances and creates a time constant:

$$\tau_W \approx R_{WB} \times C_W.$$

The feedback network of the amplifier is frequency-compensated for  $\tau_{SEGM} \approx \tau_W$ . Thus, you can calculate the value of  $R_{WB}$  as 600 $\Omega$ , meaning that the voltage gain of the amplifier,  $A_v$ , is 32.3. For gains higher than 32.3, the effect of  $C_W$  becomes negligible, and you need not bother about amplifier stability. To suppress the derivative behavior of the amplifier for gain values of two to 32.3, you can add a 40-pF compensating capacitor in parallel to feed back part of the potentiometer. The amplifier thus has an integrating character for all gains down to a value of two.

You fetch the divisor,  $Y$ , which is a digital-data word,  $D$ , through a stan-




**Figure 1** The resistive DAC-potentiometer forming the feedback for an op amp controls the op amp's gain as inversely proportional to the digital-input-data word. The circuit thus becomes a two-quadrant divider.

dard SPI (serial-peripheral interface). After power-on, you must initially neutralize the write-in protection of the resistive DAC. You have to first program the control bit  $C_1$  to the value of one, whereas it is zero by default. You achieve this task by clocking in the word containing  $C_3$ ,  $C_2$ ,  $C_1$ , and  $C_0$ ,

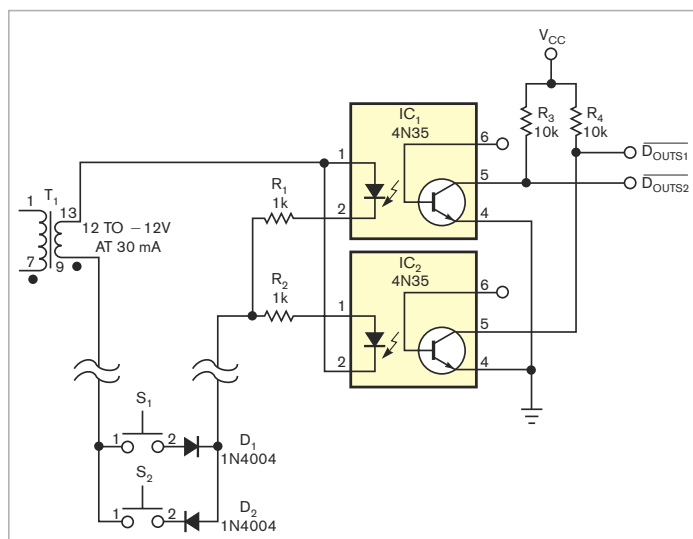
which equals 0110, and you put the desired  $C_2$  and  $C_1$  values at data positions  $D_2$  and  $D_1$ . After performing these steps, you change the wiper position in which the control bit is  $C_3$ ,  $C_2$ ,  $C_1$ , and  $C_0$ , which equals 0001, and the data bits,  $D_9$  to  $D_0$ , represent the gain as  $1024/D$ . **EDN**

## Connect two buttons with just two wires

Fikret Yilmaz, Mobil Elektronik, Istanbul, Turkey

 Sometimes, you need to read the status of pushbuttons that are as much as 5m away from your electronic circuit. That task is easy if you have just one button. You simply design a constant-current source, connect the current line from your button, and measure the current in the line. If you press the button, current flows through it. Otherwise, current does not flow.

Problems occur, however, when you need to read two or more buttons. Several approaches to this problem are available. For example, you could use an RS-485 interface with two wires for communication and two for power. Alternatively, you could use a single-wire connection



**Figure 1** You can connect two buttons using diodes.



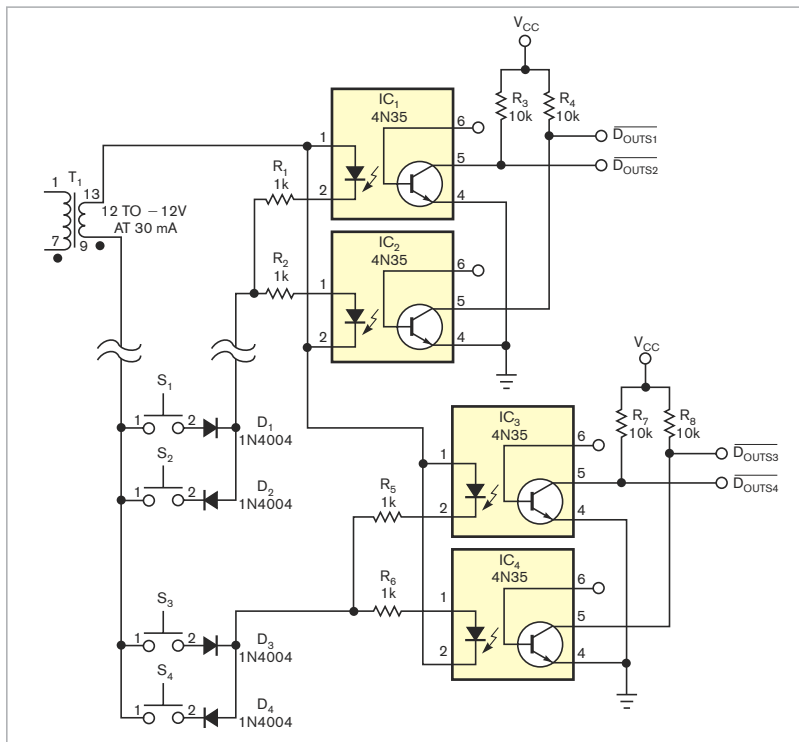


Figure 2 By adding a third wire, you can connect four pushbutton switches.

with one wire for communication and two for power. Another option is to use separate wires for each button. In that case, you would use one more wire than there are buttons. Finally, you could use a POE (power-over-Ethernet) approach, employing four wires for communication and power. All of these approaches require a button reader or a controller, which you must program, adding complexity and cost.

The circuit in **Figure 1** shows you how to connect two buttons using diodes. Because the diodes steer the current, the circuit needs just two wires. On a positive cycle from the transformer secondary and with switch  $S_2$  closed, current flows through  $IC_1$ ,  $R_1$ , and  $D_2$ . Thus, output  $D_{OUTS2}$  pulls low. Conversely, if  $S_1$  closes on a negative cycle, then current flows through  $D_1$  to  $R_1$  and  $IC_2$ , which pulls  $D_{OUTS1}$  low. The circuit in **Figure 2** extends the concept to four pushbutton switches by adding a third wire. **EDN**

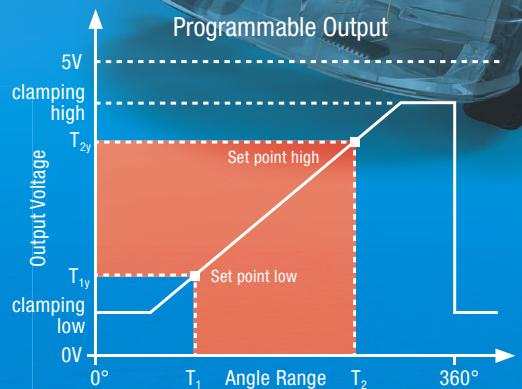
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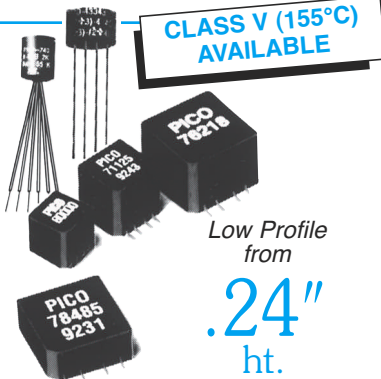
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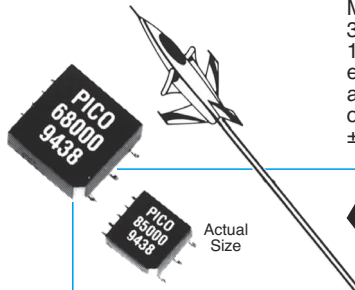


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These pulse transformers manufactured to MIL-STD-1553. COMMAND/ RESPONSE MULTI-PLEX DATA BUS requirements. They also are manufactured to MIL-PRF-21038/27 specifications and are designed to meet MAC AIR SPECIFICATIONS A3818, A5690, A5232, and A4905. All of these transformers exhibit superior electrical performance. Common mode rejection ratio is greater than 45dB at 1 MHz. Input impedance is greater than 3000 ohms over the band from 75 kHz to 1MHz at 1V rms. This series possesses exceptional waveform integrity: Rise time and fall time is less than 100 nanoseconds. Overshoot and ringing is less than  $\pm 1V$  peak. Droop is less than 20%.



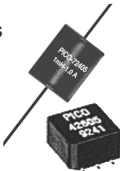
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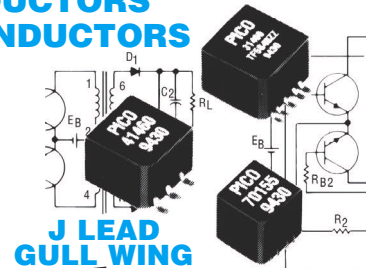
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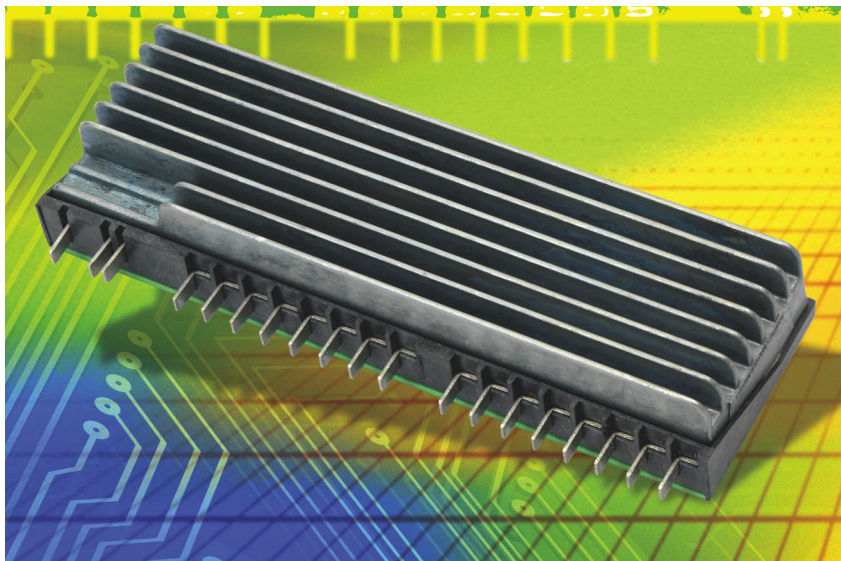
# productroundup

## POWER SOURCES

### Offline BCM arrays include a vertically mounted heat sink

Claiming 95% efficiency, the 650W, vertically mounted VI Brick BCM arrays provide isolation and conversion from 380V to 12 or 48V. Aiming at front-end applications, the devices have 352 and 384V nominal voltages and 11, 12, 44, and 48V-dc output voltages. The modules yield 290W/in.<sup>3</sup> power density and fast transient response. The BCM buses offline power to the motherboard and converts it to 12 or 48V, minimizing distribution losses and reducing conversion steps and overall cost. Devices in the VI Brick BCM-array family cost \$109 each.

**Vicor Corp**, [www.vicorpower.com](http://www.vicorpower.com)



### Triple-output dc/dc module includes switch-mode and linear regulators

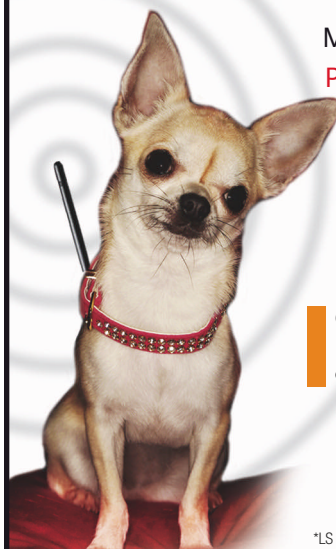
The LTM4615 triple-output dc/dc  $\mu$ Module regulator system contains two 4A switch-mode regulators and a 1.5A low-dropout linear regulator. The switching regulators have an adjustable 0.8 to 5V output voltage and regulate three outputs at 1.5, 4, and 4A or two outputs at 1.5 and 8A while operating from one, two, or three input supplies. The regulator system features short-circuit and overtemperature protection and provides a  $\pm 2\%$  total dc-output error for switch-mode regulators and  $\pm 1\%$  error for low-dropout linear regulators. Claiming 90% efficiency, the device operates over a  $-40$  to  $+125^\circ\text{C}$  temperature range. Available in a  $15 \times 15 \times 2.8$ -mm LGA package, the LTM4615 triple-output regulator costs \$17.20 (1000).

**Linear Technology Corp**, [www.linear.com](http://www.linear.com)

### Switching regulator provides alternative to linear regulators

The 96%-efficient, 0.5A V78XX-500-SMT dc-switching-regulator series provides a high-performance alternative to linear regulators. Features include a 4.5 to 28V-dc input range; 3.3, 5, 12, and 15V-dc regulated output voltage; 500-mA output current;  $-40$  to  $+75^\circ\text{C}$  temperature range at 100% load; and 60% load derating at  $85^\circ\text{C}$ . The converter provides short-circuit protection, thermal shutdown, 10-mV p-p

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# productroundup

## POWER SOURCES

typical ripple and noise, and a 2 million-hour MTBF. Measuring 15.24×8.5×7 mm, devices in the surface-mount V78XX-500-SMT dc-switching-regulator series cost \$8.24 each.

**V-Infinity, [www.v-infinity.com](http://www.v-infinity.com)**

### 10A synchronous buck converter has integrated FETs

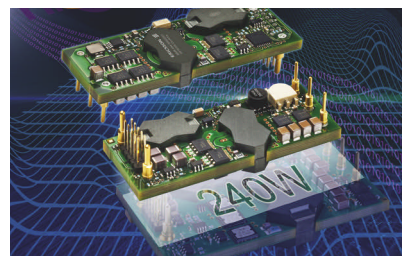
Combining a 10A synchronous buck converter with integrated FETs, the 1-MHz TPS51315 dc/dc switcher uses a D-Cap Mode control scheme, allowing fast transient response and reducing the required number of external output capacitors by 32%. The converter meets Energy Star/90 Plus

guidelines using an auto-skip mode and an Eco-mode light-load-control scheme, achieving an improved efficiency across the entire load range. Additional features include a 3 to 14V input voltage, and a 0.75 to 5.5V output-voltage range enables flexible design in 3.3, 5, and 12V power systems. Available in a 5×7-mm QFN package, the TPS51315 dc/dc switcher costs \$3.80 (1000).

**Texas Instruments, [www.ti.com](http://www.ti.com)**

### 240W one-eighth-brick module provides digital interface

Allowing monitoring using a PM-Bus interface, the BMT454 eighth-brick family delivers 240W and a 36 to



75V input-voltage range. The devices are 95% efficient at 53V input and 12V output at 20A full loads. They target information- and communication-technology applications requiring 48V power. These applications include radio base stations, servers, and routers. The devices also suit use as intermediate-bus converters with regulators or as dc/dc modules powering hard drives and fans. The modules feature a 1500V-dc input-to-output isolation fig-

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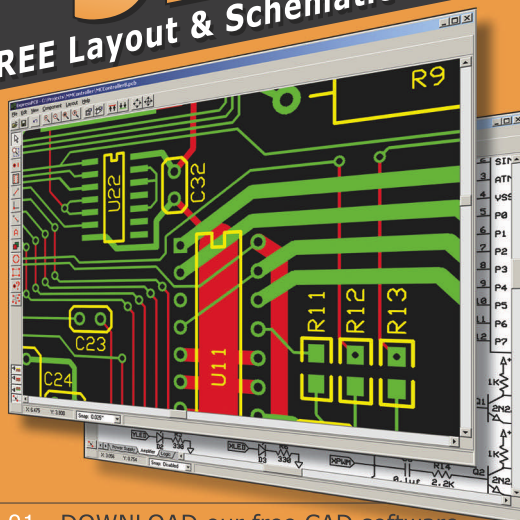
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ure, allow output-voltage adjustments between 8.1 and 13.2V with a  $\pm 2\%$  output tolerance, and have 18W/cm<sup>2</sup> power density. Available in 9V/20A, 12V/20A, and 12V/2A models without a digital interface, the BMR454 costs \$37 (10,000).

**Ericsson Power Modules,**

[www.ericsson.com](http://www.ericsson.com)

## 15W converters come in open-frame and shielded-metal-case options

 The fully isolated, 15W PXA open-frame and PXB shielded-metal-case dc/dc converters provide 88% efficiency and have a  $-40$  to  $+85^\circ\text{C}$  operating temperature. The


PXA series has single-output models with 24V nominal inputs and 48V dc in 2-to-1 and wide 4-to-1 versions. The PXB series comes in single- and dual-output models with 12V-dc nominal inputs in a 2-to-1 version and 24 and 48V-dc inputs in 2-to-1 and wide 4-to-1 versions. Single-output voltages include 3.3, 5, 12, and 15V dc, and the PXB series offers dual-output models providing  $\pm 5$ ,  $\pm 12$ , and  $\pm 15\text{V-dc}$  outputs. Standard models include remote on/off and output adjustment; single-output models and devices with over-voltage and overcurrent/short-circuit protection are also available. Measuring 1x1 in. each, devices in the PXA and PXB series cost \$28 (500).

**TDK-Lambda Corp,**

[www.us.tdk-lambda.com](http://www.us.tdk-lambda.com)

## INTEGRATED CIRCUITS

### Op amp uses EMI-suppression filters

 Consuming 560nW, the LPV521 op amp suits wireless remote sensors, power-line monitoring, and micropower oxygen and gas sensors. Features include a 1.6 to 5.5V voltage range with a 0.4- $\mu\text{A}$  maximum supply current, a maximum 1-mV input offset voltage, and a 3.5- $\mu\text{V}/^\circ\text{C}$  input offset-voltage drift. The op amp comes with EMI-suppression filters, reducing RFI from external sources. Available in a five-pin SC-70 package, the LPV521 op amp costs 65 cents (1000).

**National Semiconductor,**

[www.national.com](http://www.national.com)


perature coefficient, and an 800-nA maximum supply current. The voltage reference sources or sinks as much as 10 mA of load current with 50 mV of dropout; the devices require no output-bypass capacitor for most applications. The devices have an eight- to 12-week leadtime and come in three-lead SOT-23 packages. The CAT8900 voltage reference comes in  $\pm 5$ -,  $\pm 2.5$ -,

$\pm 1$ -, and  $\pm 0.5$ -mV initial accuracy grades and costs 60 cents, 92 cents, \$1.55, and \$2.44 (1000), respectively.

**On Semiconductor,**

[www.onsemi.com](http://www.onsemi.com)

### Voltage-reference ICs come in multiple accuracy grades

 The CAT8900 voltage reference aims at handheld medical devices, high-resolution ADCs and DACs, and precision-regulator systems. The device offers 1.024, 1.2, 1.25, 1.8, 1.048, 1.5, 2.6, 3, and 3.3V voltage-reference options; custom voltages are available on request. The device provides 0.02% initial accuracy at  $\pm 0.5$  mV, a 20-ppm/ $^\circ\text{C}$  tem-

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## EDN ADVERTISER INDEX

Company	Page	Company	Page
Achronix Semiconductor	C-3	Mentor Graphics	12
Agilent Technologies	C-2	Micro Crystal	35
	21, 29	Mill Max Manufacturing Corp	9
Analog Devices Inc	17	Mouser Electronics	4
austriamicrosystems AG	50	National Instruments	2
Bergquist Co	24	National Semiconductor	44
Coilcraft	7	Pico Electronics	23
Digi-Key Corp	1		34, 52
Express PCB	54	Renesas Technology Corp	37
International Rectifier Corp	5	Samsung Electro-Mechanics	42
Keil Software	33	Silicon Labs	38
Linear Technology Corp	C-4	Tadiran Electronic Industries	8
LPKF Laser & Electronics	36	Trilogy Design	55
LS Research	53	Vicor	41, 43
Magna-Power Electronics Inc	28	Xilinx Inc	51
MathWorks Inc	19		
Maxim Integrated Products	10, 11		
Memory Protection Devices	54		

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## Lightning strikes sewage setup



In early 1988, we had finished the start-up of a brand-new SCADA (supervisory-control-and-data-acquisition) system at the water-and-sewer utility where I work. It was summer, and we were busy repairing the damage from frequent thunderstorms. A co-worker, George, was supposed to provide postmortem repair and analysis of the RTU (remote-telemetry-unit) processor boards. Most of the 1-foot-square, multilayer processor boards had obvious scorch marks from lightning damage. We'd typically see a burned switching-power-supply module, PCB (printed-circuit-board) burns at the phone-line interface, or burns on an analog-input card. We'd then take a closer look at each of the sites where these boards originated and try to improve the situation through more careful grounding, better surge suppressors, or another means.

One morning, I noticed that George had set aside a few RTU processor cards. When I asked about it, he told me that they were malfunctioning but that he'd been having a hard time with figuring out what was wrong, so he'd set them aside to work on when he had time. "I

just repaired this one over here," he said. "It was a single blown 74HC00 gate; the other three in the same chip were just fine." I asked where another similar card had come from. "You're going to love this," he said, "All of these problem cards, except for one, are from the Cabin John interceptor." I walked away, befuddled.

I made a detour in my travels later that week to take a look at the Cabin John interceptor, a waste-water metering vault. Resembling a small brick out-house, it sat at the bottom of a valley in the woods. The RTU processor's only purpose at that site was to gather flow data from a large venturi tube, which

measures fluid pressures and velocities, in the vault below the building. This flow meter was important because it was a change-of-custody billing meter. The saying "sewage flows downhill" isn't just an expression; it's also a fact of life. The sewage in this area was headed for a plant in another jurisdiction.

The only two points of data coming from the site were flow and a loss-of-ac-power alarm. The RTU processor was in a robust fiberglass box. At the back of the box, all the PCBs mounted flat on a grounded steel plate with ¼-in. standoffs and isolated screws. The setup also included an I/O card, the processor card, a battery-charge controller board, some terminal strips, an ac circuit breaker, and the 928/952-MHz telemetry radio. A 100-foot tower stood next to the building to get the antenna above the tree line.

The installation gathered the flow data from a 4- to 20-mA-current-loop pressure transmitter next to the cabinet. The pressure-transducer electronics, batteries, and PCBs were isolated from ground. Sure that George must have been wrong about something, I went back to his shop. He had set aside a few more cards, all with different failures.

The next morning, as I stumbled into the shower, I had a flash of insight: Maybe lightning was striking the tower and causing the ground potential of the backplate to rise. The board was quite close to the backplate. Perhaps a static charge was forming between the grounded metal backplate and the isolated RTU processor. A small arc could be destroying the weakest chips.

I got to work early and snagged some 1-in.-long nylon screws and standoffs from the maintenance shop. Replacing the ¼-in. screws with the longer ones protected the isolated board from random chip damage, fixing the problem, and we haven't seen failures of this sort since. **EDN**

*Jacob Brodsky is a control-system engineer with the Washington Suburban Sanitary Commission (Laurel, MD).*

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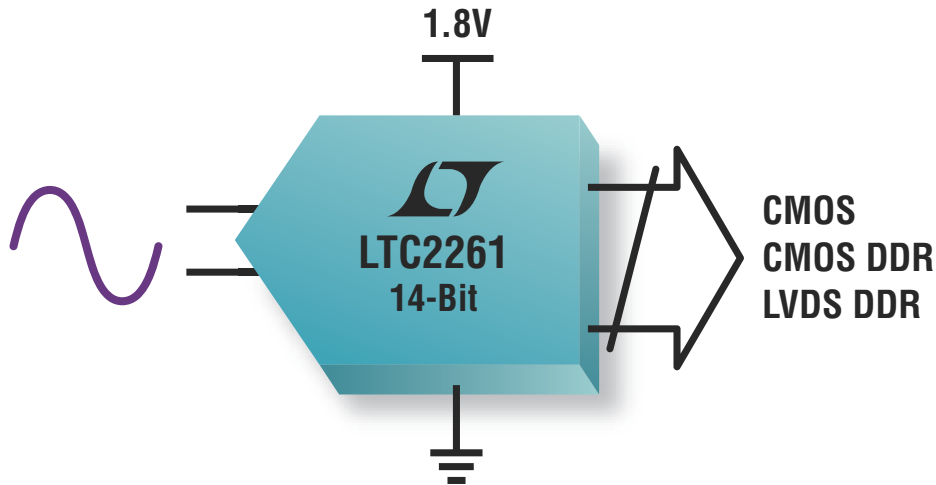
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